

ELECTRICAL ENGINEERING

POWER ELECTRONICS



Comprehensive Theory
with Solved Examples and Practice Questions





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Power Electronics

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CONTENTS

Power Electronics

CHAPTER 1

Introduction1-6

- 1.1 Power Electronics..... 1
- 1.2 Classification of the Power Semiconductors..... 4

CHAPTER 2

Power Semi-Conductor Diode and Transistor7-27

- 2.1 Basic Semiconductor Physics
 - Important Concepts..... 7
- 2.2 Basic Structure and I-V Characteristics..... 7
- 2.3 Power Bipolar Junction Transistor : (Power BJT) 11
- 2.4 Power Mosfet..... 17
- 2.5 Insulated Gate Bipolar Transistor (IGBT) 22
 - Objective Brain Teasers* 25
 - Conventional Brain Teasers* 25

CHAPTER 3

Diode Circuits and Rectifiers..... 28-56

- 3.1 Diode Circuits..... 28
- 3.2 Performance Parameters..... 31
- 3.3 Single-Phase Diode Halfwave Rectifier..... 32
- 3.4 Single-Phase Fullwave Diode Rectifier..... 42
- 3.5 Three-Phase Rectifier..... 45
 - Objective Brain Teasers* 51
 - Conventional Brain Teasers* 54

CHAPTER 4

Thyristors..... 57-91

- 4.1 Introduction..... 57
- 4.2 Silicon Controlled Rectifier (SCR) 57
- 4.3 Structural Modification of the Device 68
- 4.4 Heating and Cooling of SCR..... 69
- 4.5 Series and Parallel Operation of SCR..... 69
- 4.6 Firing Circuits for Thyristors..... 73
- 4.7 Other Members of Thyristor Family..... 77
 - Objective Brain Teasers* 85
 - Conventional Brain Teasers* 88

CHAPTER 5

Thyristor Commutation Techniques.....92-104

- 5.1 Introduction..... 92
 - Objective Brain Teasers* 104

CHAPTER 6

Phase Controlled Rectifiers 105-163

- 6.1 Introduction..... 105
- 6.2 Firing Angle..... 105
- 6.3 1- ϕ Half-Wave Controlled Rectifier with R-Load 105
- 6.4 1- ϕ Halfwave Rectifier with RL-Load 109
- 6.5 1- ϕ Halfwave Rectifier with R-L Load and Free-Wheeling Diode 110
- 6.6 Single Phase (1- ϕ) Halfwave Rectifier with RLE Load 112

6.7	1- ϕ Fullwave Bridge Rectifier with R-Load	116
6.8	1- ϕ Full Wave Rectifier With RL-Load	117
6.9	Inverter Mode of Operation of 1- ϕ Full Converter .	123
6.10	1- ϕ Fullwave Semi-converter with RLE Load (or) 1- ϕ Full Wave Half Controlled Rectifier with Free Wheeling Diode	126
6.11	3- ϕ Controlled Half Wave Rectifier	135
6.12	Three-Phase Halfwave Rectifier with R-L Load	137
6.13	3- ϕ Full Converter (or) 3- ϕ Full Wave Rectifier	138
6.14	3- ϕ Fullwave Semi-Converter with RLE Load and Freewheeling Diode	144
6.15	Effect of Source Inductance (L_s) : One Pulse Converter	147
6.16	Effect of Source Inductance : L_s : Two Pulse Converter	148
6.17	Dual Converter	152
	<i>Objective Brain Teasers</i>	155
	<i>Conventional Brain Teasers</i>	160

CHAPTER 7

Choppers.....	164-206
7.1	Definition 164
7.2	Principle of Operation of Step Down Chopper 164
7.3	Principle of Operation of Step-Up Choppers..... 168
7.4	Principle of Operation of Step up/Step down Choppers..... 171
7.5	Switching Mode Regulators 173
7.6	First-Quadrant or Type-A Chopper 181
7.7	Second-Quadrant or Type-B Chopper..... 182
7.8	Type-D Chopper (or) Two Quadrant Type-B Chopper..... 183
7.9	Four Quadrant Chopper or Type-E Chopper..... 183
7.10	Steady State Analysis of Type A Chopper..... 184
7.11	Theory of Tank Circuit..... 189
	<i>Objective Brain Teasers</i> 195
	<i>Conventional Brain Teasers</i> 199

CHAPTER 8

Inverters	207-246
8.1	1- ϕ Half Bridge Inverters..... 207
8.2	1- ϕ Full Bridge Inverters 209
8.3	Fourier Analysis of 1- ϕ Inverter Output Voltage 213
8.4	Pulse-Width Modulation 217
8.5	3- ϕ Bridge Inverter..... 226
8.6	3- ϕ 120° Mode VSI..... 229
8.7	Current Source Inverter (CSI) 231
	<i>Objective Brain Teasers</i> 234
	<i>Conventional Brain Teasers</i> 240

CHAPTER 9

Resonant Converters	247-258
9.1	Introduction..... 247
9.2	Zero-Current-Switching Resonant Converters..... 249
9.3	L-Type ZCS Resonant Converter 249
9.4	M-Type ZCS Resonance Converter (DC–DC) 251
9.5	Zero-Voltage Switching Resonant Converters (DC-DC) 254
9.6	Comparisons between ZCS and ZVS Resonant Converters 257

CHAPTER 10

Power Semiconductor Drives	259-281
10.1 DC Drives	259
10.2 AC Drives.....	270
10.3 Static Kramer Drive.....	272
10.4 Static Scherbius Drive	272
<i>Objective Brain Teasers</i>	<i>274</i>
<i>Conventional Brain Teasers</i>	<i>277</i>

CHAPTER 11

High Frequency Inductors
and Transformers 282-285

11.1 Design of Magnetic Components for Power
Electronics 282

11.2 Magnetic Material and Cores..... 282

11.3 Hysteresis Loss 282

11.4 Skin Effect Limitations..... 283

11.5 Eddy Current Loss in Laminated Cores 284

11.6 Copper Windings 284

11.7 Winding Loss Due to DC Resistance of Windings... 284

11.8 Skin Effect in Copper Windings..... 284

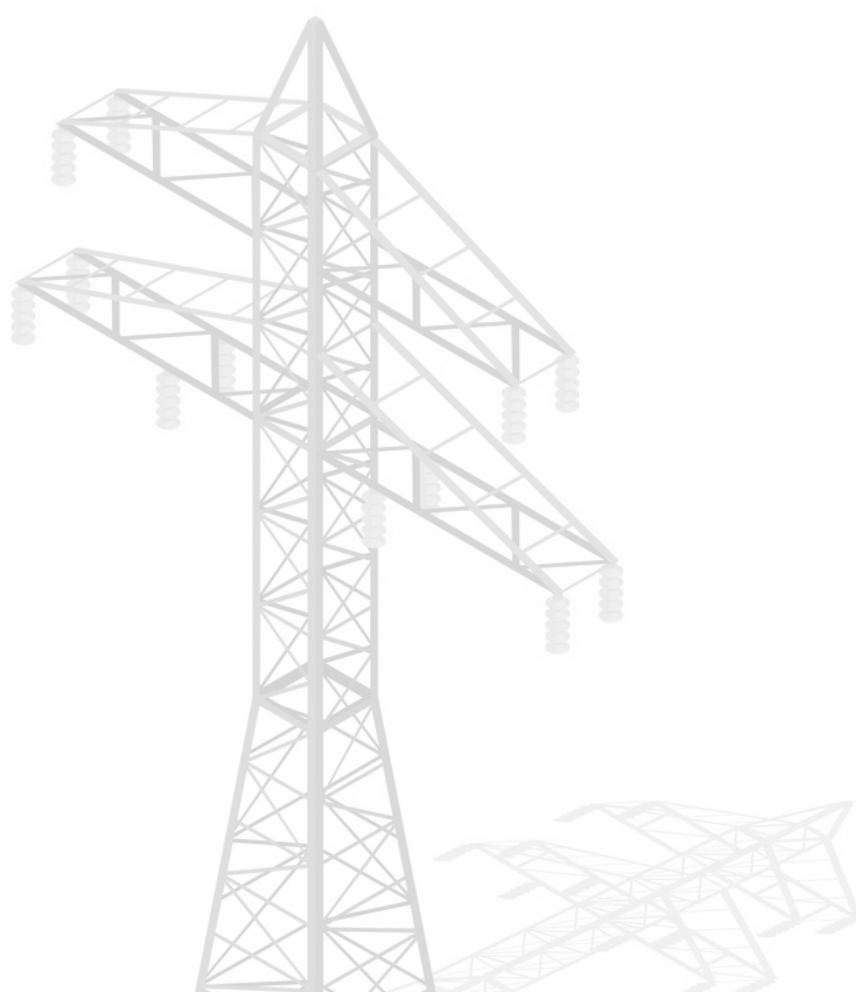
11.9 Thermal Considerations 285

CHAPTER 12

Switched Mode Power Supply 286-291

12.1 Switched Mode Power Supply (SMPS) 286





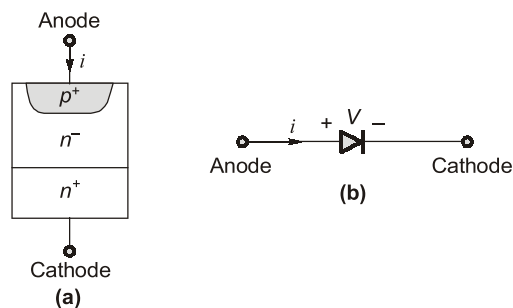
Power Semi-Conductor Diode and Transistor

2.1 BASIC SEMICONDUCTOR PHYSICS IMPORTANT CONCEPTS

- Current in a semiconductor is carried by both electrons and holes.
- Electron and holes move by both drift and diffusion.
- Intentional doping of the semiconductor with impurities will cause the density of holes and electrons to be vastly different.
- The density of minority carriers increases exponentially with temperature.
- A pn junction can be formed by doping one region n -type and the adjacent region p -type.
- A potential barrier is set up across a pn junction in thermal equilibrium that balances out the drift and diffusion of carriers across the junction so that no net current flows.
- In reverse bias a depletion region forms on both sides of the pn junction and only a small current can flow by drift.
- In forward bias large numbers of electrons and holes are injected across the pn junction and large currents flow by diffusion with small applied voltages.
- Large numbers of excess electron-hole pairs are created by impact ionization if the electric field in the semiconductor exceeds a critical value.
- Avalanche breakdown occurs when the reverse-bias voltage is large enough to generate the critical electric field E_{BD} .

2.2 BASIC STRUCTURE AND I-V CHARACTERISTICS

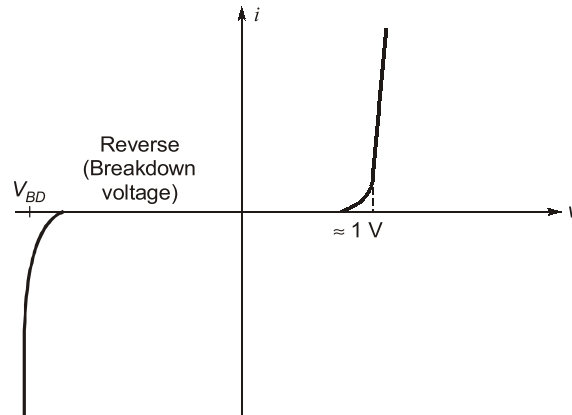
The practical realization of diode for power application is shown below :



It consists of a heavily doped n -type substrate on top which is grown a lightly doped ' n -type' epitaxial layer of specified thickness. Finally, the p - n junction is formed by diffusing in a heavily doped p -type region that forms the anode of the diode.

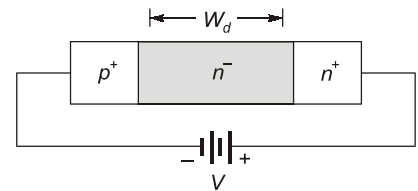
The n^- layer which is often termed the drift region, is the prime structural feature not formed in low power diodes. Its function is to absorb the depletion layer of the reverse biased $p^+ n^-$ junction.

This relatively long lightly doped region would appear to add significant ohmic resistance to the diode when it is forward biased.



The current grows linearly with the forward bias voltage rather than exponentially.

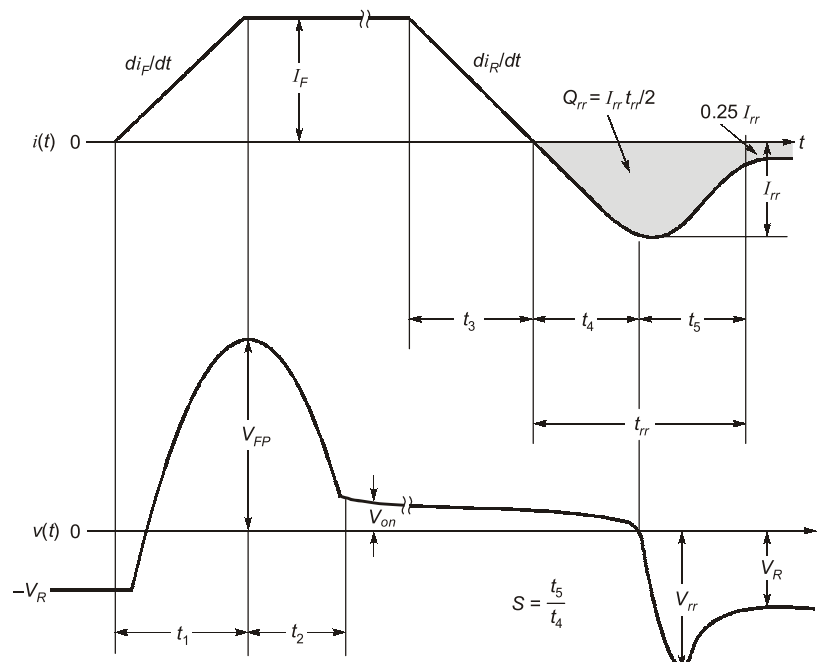
In reverse bias only a small leakage current, which is independent of the reverse voltage, flows until the reverse break down voltage V_{BD} is reached. When breakdown is reached the voltage appears to remain essentially constant while the current increases dramatically.



If the length W_d of the lightly doped region is longer than the depletion layer width at breakdown, then the structure is termed a non punch through diode, that is, the depletion layer has not reached through (or punched through) the lightly doped drift region and reached the highly doped n^+ substrate.

Two basic facts; first, large breakdown voltages require lightly doped junctions, at least on one side. Second, the drift layer in the diode must be fairly long in high voltage devices to accommodate the long depletion layers.

2.2.1 Switching Characteristics



A power diode requires a finite time to switch from the blocking state (reverse bias) to the on state (forward bias) and vice versa.

The features of particular interest in these waveforms are the voltage overshoot during turn on and the sharpness of the fall of the reverse current during the turn off phase.

The overshoot of the voltage during turn on is not observed with signal level diodes.

1. Turn-on Transient

The turn on portion of the diode waveform is encompassed by the times labeled t_1 and t_2 . During these intervals two physical process occur in sequence. First the space charge stored in the depletion region (located mainly in the drift region) because of the large reverse bias voltage is removed (discharged) by the growth of the forward current. When the depletion layer is discharged to its thermal equilibrium level, the metallurgical junction becomes forward biased and the injection of excess carriers across the junction into the drift region commences at time t_1 , thus marking the start of the second phase and the end of the first. During the second phase, the excess-carrier distribution in the drift region grows towards the steadily state value that can be supported by the forward diode current I_F .

NOTE: Excess carries are injected into the drift region from both ends with holes being injected from the $p^+ n^-$ junction and electrons from the $n^+ n^-$ junction.

2. Turn-off Transient

The turn off portion of the switching waveform is encompassed by the times labeled t_3 , t_4 and t_5 and is essentially the inverse of the turn on process. First the excess carriers stored in the drift region must be removed before the metallurgical junctions can become reverse biased.

Once the carriers are removed by the combined action of recombination and sweep out by negative diode currents, the depletion layer acquires a substantial amount of space charge from the reverse bias voltage and expands into the drift region from both ends (junctions).

As long as there are excess carriers at the ends of the drift region, the $p^+ n^-$ and $n^+ n^-$ junctions must be forward biased. Thus, the diode voltage will little change from its on state value except for a small decrease due to ohmic drops caused by the reverse current. But after the current goes negative and carrier sweep-out has proceeded for a sufficient time (t_4) to reduce the excess carriers density at both junctions to zero, the junctions become reverse biased. At this point the diode voltage goes negative and rapidly acquires substantial negative values as the depletion regions from the two junctions expand into the drift region towards each other.

The diode current ceases its growth in the negative direction and quickly falls, becoming zero after a time t_5 .

The reverse current has its maximum reverse value, I_{rr} , at the end of the t_4 interval.

3. Reverse Recovery

The time interval $t_{rr} = t_4 + t_5$ shown in the graph is often termed the reverse recovery time. Its characteristics are important in almost all power electronic circuits where diode are used.

t_{rr} = reverse recovery time; Q_{rr} = reverse recovery charge

$\frac{di_R}{dt}$ = rate of change of reverse current

S = snappiness factor or softness factor

These quantities are inter related to each other.

We note that I_{rr} can be written as : $I_{rr} = \frac{di_R}{dt} \times t_4$

$$\therefore s = \frac{t_5}{t_4}$$

$$t_4 = t_{rr} - t_5 = \frac{t_{rr}}{s+1}$$

$$\therefore I_{rr} = \frac{di_R}{dt} \times \frac{t_{rr}}{s+1}$$

$$Q_{rr} \equiv \frac{1}{2} I_{rr} t_{rr}$$

So that,

$$Q_{rr} = \frac{di_R}{dt} \frac{t_{rr}^2}{2(s+1)}$$

Reverse recovery time,

$$t_{rr} = \sqrt{\frac{2Q_{rr}(1+s)}{\left(\frac{di_R}{dt}\right)}}; \quad I_{rr} = \sqrt{\frac{2Q_{rr}\left(\frac{di_R}{dt}\right)}{(s+1)}}$$

The charge Q_{rr} represents the portion of the total charge Q_F (the charge stored in the diode during forward bias), which is swept out by the reverse current and not lost to internal recombination. Most of Q_F is stored in the drift region.

EXAMPLE : 2.1

A power diode is in the forward conduction mode and the forward current is now decreased. The reverse recovery time of the diode is t_r and the rate of fall of the diode current is di/dt . What is the stored charge?

Solution :

From figure,

$$I_{RM} = t_a \frac{di}{dt}$$

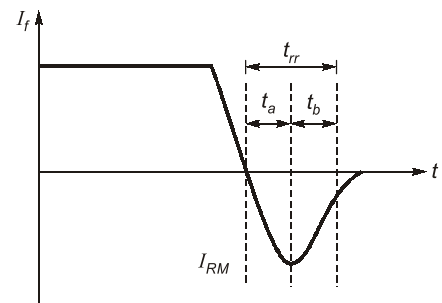
Assuming reverse recovery characteristics to be triangular,

Storage charge Q_R

$$Q_R = \frac{1}{2} I_{RM} t_{srr} = \frac{1}{2} \left(t_a \frac{di}{dt} \right) t_{rr}$$

if $t_a \approx t_{rr}$,

$$Q_R = \frac{1}{2} \left(\frac{di}{dt} \right) t_{rr}^2$$



Reverse Recovery Characteristic

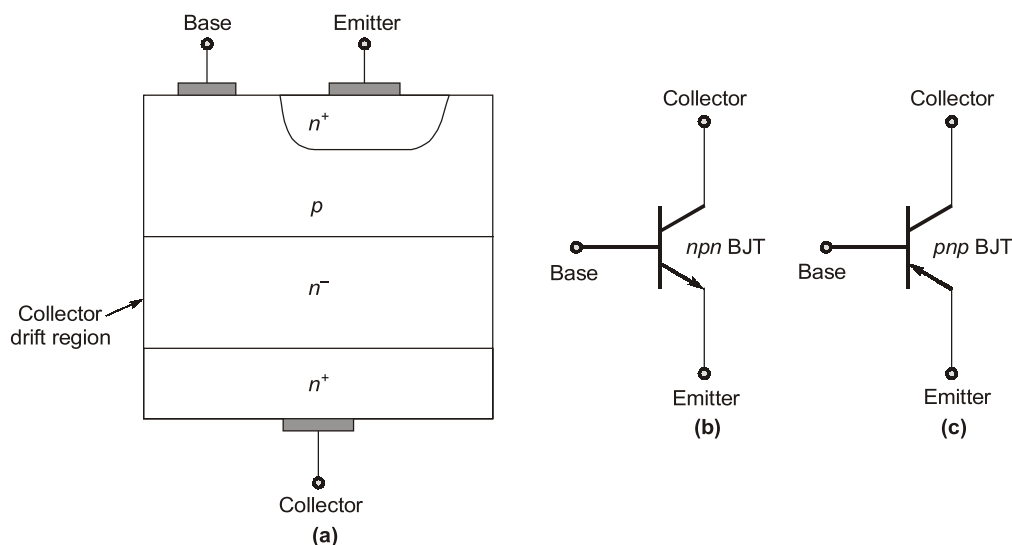
Points to Remember in Power Semiconductor Diodes

- Power diodes are constructed with a vertically oriented structure that includes a ' n^- ' drift region to support large blocking voltages.
- The breakdown voltage is approximately inversely proportional to the doping density of the drift region, and the required minimum length of the drift region scales with the desired breakdown voltage.
- Achievement of large breakdown voltages requires special depletion layer boundary shaping techniques.

- Conductivity modulation of the drift region in the on state keeps the losses in the diode to manageable levels even for large on-state currents.
- Low on-state losses require long carrier lifetimes in the diode drift region.
- Minority-carrier devices have lower on-state losses than majority-carrier devices such as MOSFETs at high blocking voltage ratings.
- During the turn-on transient the forward voltage in a diode may have a substantial overshoot, on the order of tens of volts.
- Short turn-off times require short carrier lifetimes, so a trade-off between switching times and on-state losses must be made by the device designer.
- During turn-off, fast reverse recovery may lead to large voltage spikes because of stray inductance.
- The problems with the reverse-recovery transient are most severe in diodes with large blocking voltage ratings.
- Schottky diodes turn on and off faster than pn -junction diodes and have no substantial reverse-recovery transient.
- Schottky diodes have lower on-state losses than pn -junction diodes but also have low breakdown voltage ratings, rarely exceeding 100 V.

2.3 POWER BIPOLAR JUNCTION TRANSISTOR : (POWER BJT)

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power Bipolar Junction Transistor (BJT) must have a substantially different structure than its logic level counterpart. The modified structure leads to significant differences in I-V characteristics.



In most power applications, the base is the input terminal, the collector is the output terminal, and the emitter is common between input and output (the so called common emitter configuration). A pnp transistor, whose circuit symbol is shown above, would have the opposite type of doping in each of the layers shown in the figure.

NOTE: nnp transistors are much more widely used than pnp transistor as power switches.

The vertical structure is preferred for power transistors because it maximizes the cross sectional area through which the current in the devices is flowing. This minimizes the on state resistance and thus the power

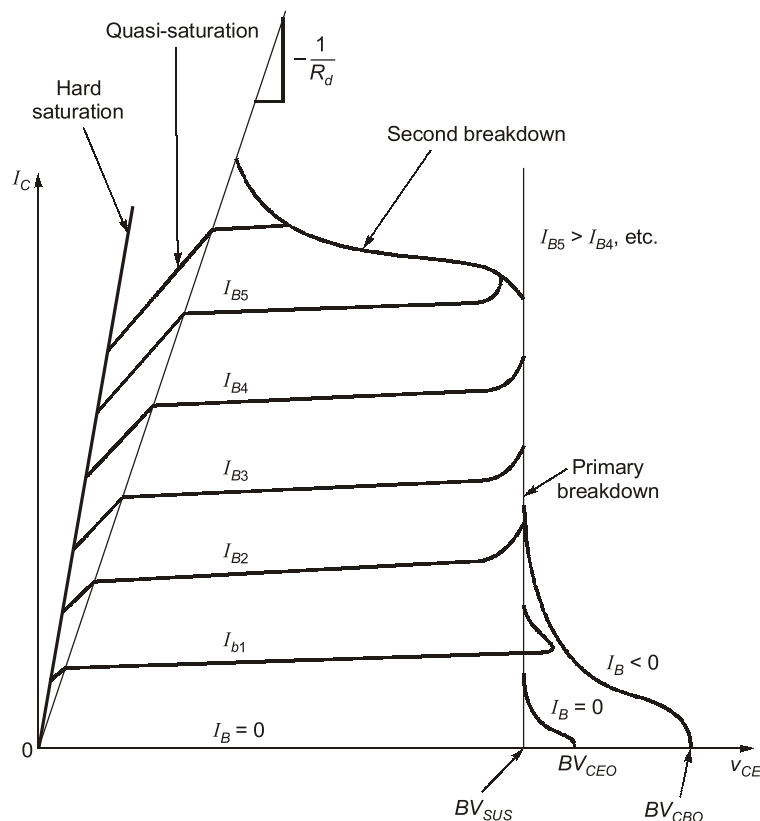
dissipation in the transistor. In addition, having a large cross sectional area minimizes the thermal resistance of the transistor, thus also helps to keep power dissipation problems under control. The doping levels in each of the layers and the thickness of the layers have a significant effect on the characteristics of the device. The doping in the emitter layer is quite large, where as the base doping is moderate. The n^- region that forms the collector half of the $C-B$ (collector base) junction is usually termed the collector drift region and has a light doping level. The n^+ region that terminates the drift region has a doping level similar to that found in the emitter.

NOTE: The thickness of the drift region determines the breakdown voltage of the transistor.

I-V Characteristics

The output characteristics (I_C versus V_{CE}) of a typical npn power transistor are shown above. The various curves are distinguished from each other by the value of the base current. There is a maximum collector-emitter voltage that can be sustained across the transistor when it is carrying substantial collector current. This voltage is usually labeled BV_{SUS} . In the limit of zero base current, the maximum voltage between collector and emitter that can be sustained increase somewhat to a value labeled BV_{CEO} , the collector emitter breakdown voltage when the base is open circuited. This voltage is measure of the transistor's voltage standoff capability because usually the only time the transistor will see large voltages, when the base current is zero and the BJT is in cut-off.

The voltage BV_{CBO} is the collector base breakdown voltage when the emitter is open circuited.



The region labeled primary breakdown is due to conventional avalanche breakdown of the $C-B$ junction and attendant large flow of current. This region of characteristics is to be avoided because of the large power dissipation that clearly accompanies such breakdown.

The major difference between the $i-v$ characteristics of a power transistor and those of a logic level transistor is the region labeled Quasi-Saturation on the power transistor characteristics.

Quasi-Saturation

To understand the phenomenon of quasi saturation, the collector drift region should be considered. It is assumed that the transistor is initially in the active region and now base current is allowed to increase.

There is a simultaneous increase in the voltage drop in the drift region as a result of its ohmic resistance because of the increase in I_C .

A very large number of electrons are supplied to the C - B junction via injection from the emitter and subsequent diffusion across the base. As this excess carriers build up in the drift region begins to occur, the quasi saturation region of the i - v characteristics is entered.

The ohmic resistance of the drift region is R_d , then the boundary between the quasi saturation region and the active region is given by

$$I_C = \frac{V_{CE}}{R_d}$$

As the injected carriers increase, the drift region is gradually shorted out and the voltage across the drift region drops even though the collector current is large.

Hard saturation is obtained when the excess- carriers density reaches the other side of the drift region.

Relation Between α and β

Most of the electrons, proportional to I_E , given out by emitter, reach the collector. In other words, collectors current I_C , though less than emitter current I_E , is almost equal to I_E . A symbol α is used to indicate how close in value these two current are. Here α , called forward current gain, is defined as

$$\alpha = \frac{I_C}{I_E}$$



As $I_C < I_E$, value of α varies from 0.95 to 0.99. In transistor, base current is effectively the input current and collector current is output current. The ratio of collector (output) current I_C to base (input) current I_B is known as the current gain β .

$$\beta = \frac{I_C}{I_B}$$

Use of KCL,

$$I_E = I_C + I_B$$

NOTE: The emitter current is the largest of three currents, collector current is almost equal to, but less than, emitter current. Base current has the least value.

Dividing both sides by I_C , we get

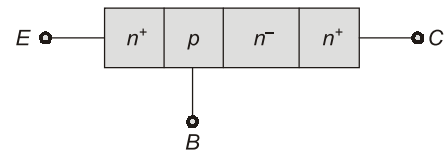
$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow \alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

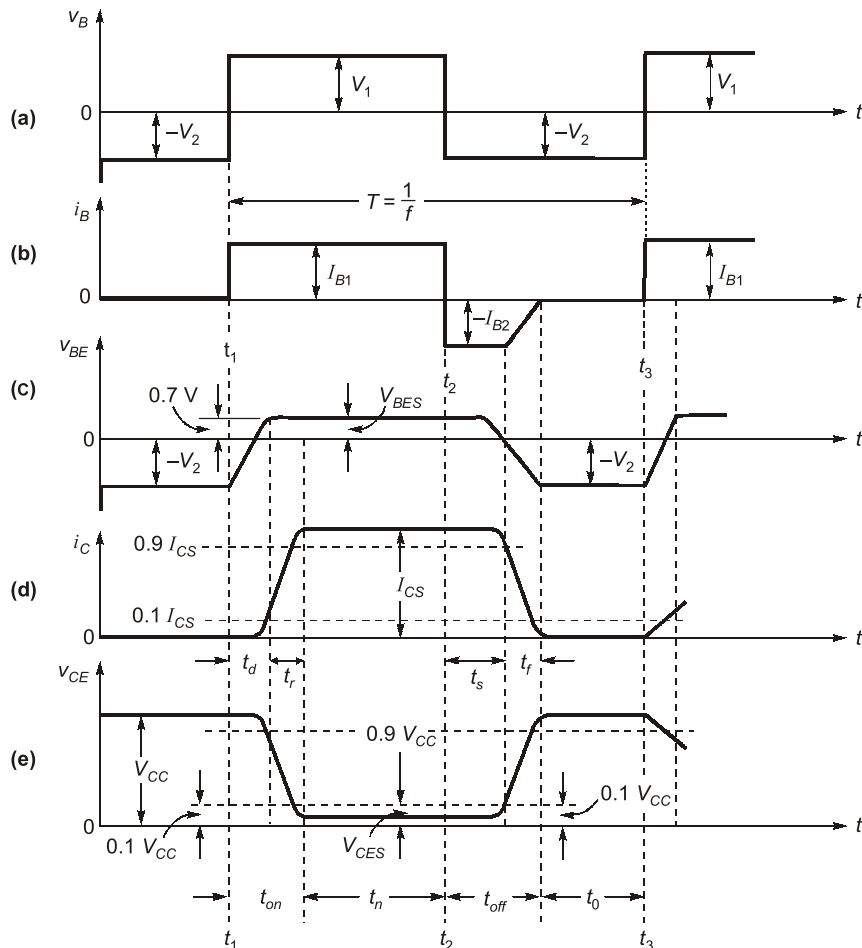
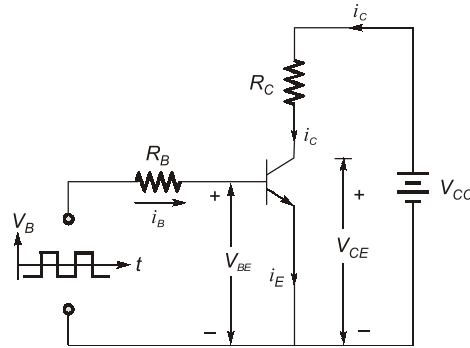
BJT Switching Performance

When input voltage V_B to base circuit is made $-V_2$ at t_0 , junction EB is reverse biased, $V_{BE} = -V_2$, the transistor is off, $i_B = i_C = 0$ and $V_{CE} = V_{CC}$.



At time t_1 , base emitter voltage V_{BE} begins to rise gradually from $-V_2$ and collector current i_C begins to rise from zero and collector-emitter voltage V_{CE} starts falling from initial value V_{CC} . After sometime delay t_d , called delay time, the collector current rises to $0.1 I_{CS}$, V_{CE} falls from V_{CC} to $0.9 V_{CC}$ and V_{BE} reaches $V_{BES} = 0.7$ V.

This delay time is required to charge the base emitter capacitance to $V_{BES} = 0.7$ V.



- (a) 1 and 2 only
(b) 1, 2 and 3 only
(c) 2, 3 and 5 only
(d) 1, 2, 3, 4 and 5

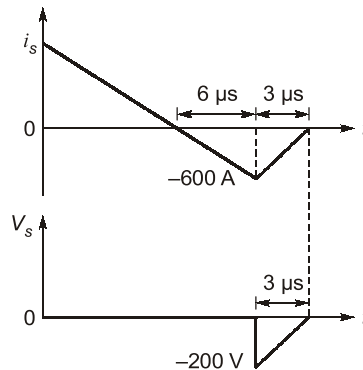
Solution : (a)

SCR, GTO and TRIAC belong to the family of thyristors, while BJT, MOSFET and IGBT belong to the family of transistors.



OBJECTIVE BRAIN TEASERS

- Q1** During turn off a thyristor, idealized voltage and current waveforms are shown below. For a triggering frequency of 50 Hz, the mean power loss due to turn off is _____ W.



1. (6)

$$\text{The power loss, } P = \frac{1}{T} \int_0^3 V_s(t) i_s(t) dt = \frac{1}{T} \int_0^3 \left(\frac{200}{3} t \right) \left(\frac{600}{3} t \right) dt = \frac{40000}{3T} \int_0^3 t^2 dt = \frac{40000}{3T} \left[\frac{t^3}{3} \right]_0^3$$

$$\text{where } T \text{ is in } \mu\text{sec} \Rightarrow T = \frac{1}{50} \times 10^6 = 20000$$

$$\text{So, } P = \frac{40000}{3 \times 20000} \left[\frac{3^3}{3} \right] = 6 \text{ Watt average power loss}$$



CONVENTIONAL BRAIN TEASERS

- Q1** A sinusoidal voltage source of $v(t) = 100 \cos(377t)$ V is applied to a non-linear load, resulting in a non-sinusoidal current which is expressed in Fourier series form as

$$i(t) = 8 + 15 \cos(377t + 30^\circ) + 6 \cos[2(377)t + 45^\circ] + 2 \cos[3(377)t + 60^\circ]$$

Determine (a) the power absorbed by the load, (b) the power factor of the load, (c) the distortion factor of the load current, (d) the total harmonic distortion of the load current.

1. (Sol)

- (a) The power absorbed by the load is determined by computing the power absorbed at each frequency in the fourier series.

$$P = (0)(8) + \left(\frac{100}{\sqrt{2}}\right)\left(\frac{15}{\sqrt{2}}\right)\cos 30^\circ + 0\left(\frac{6}{\sqrt{2}}\right)\cos 45^\circ + (0)\left(\frac{2}{\sqrt{2}}\right)\cos 60^\circ = \left(\frac{100}{\sqrt{2}}\right)\left(\frac{15}{\sqrt{2}}\right)\cos 30^\circ = 650 \text{ W}$$

- (b) The rms voltage is : $V_{\text{rms}} = \frac{100}{\sqrt{2}} = 70.7 \text{ V}$

$$\text{and the rms current is computed : } I_{\text{rms}} = \sqrt{8^2 + \left(\frac{15}{\sqrt{2}}\right)^2 + \left(\frac{6}{\sqrt{2}}\right)^2 + \left(\frac{2}{\sqrt{2}}\right)^2} = 14.0 \text{ A}$$

$$\text{The power factor is : } \text{pf} = \frac{P}{S} = \frac{P}{V_{\text{rms}} I_{\text{rms}}} = \frac{650}{(70.7)(14.0)} = 0.66$$

$$\text{Alternatively, power factor can be computed : } \text{pf} = \frac{I_{1,\text{rms}} \cos(\theta_1 + -\phi_1)}{I_{\text{rms}}} = \frac{\left(\frac{15}{\sqrt{2}}\right) \cos(0 - 30^\circ)}{14.0} = 0.66$$

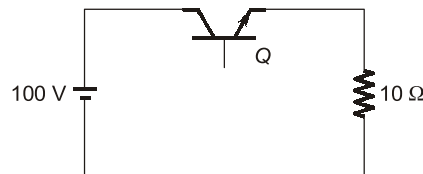
- (c) The distortion factor is computed as : $\text{DF} = \frac{I_{1,\text{rms}}}{I_{\text{rms}}} = \frac{\frac{15}{\sqrt{2}}}{14.0} = 0.76$

- (d) The total harmonic distortion of the load current is obtained as

$$\text{THD} = \sqrt{\frac{I_{\text{rms}}^2 - I_{1,\text{rms}}^2}{I_{1,\text{rms}}^2}} = \sqrt{\frac{14^2 - \left(\frac{15}{\sqrt{2}}\right)^2}{\left(\frac{15}{\sqrt{2}}\right)^2}} = 0.86 = 86\%$$

Q2 In the figure below, the transistor Q is operating at 10 kHz and 40% duty ratio. If the transistor has on-state voltage drop of 1 V and $t_{\text{on}} = t_{\text{off}} = 5 \mu\text{s}$, find its total losses during the operation.

(Assume linear rise and fall characteristics of the voltage and currents in the device during switching).

**2. (Sol)**

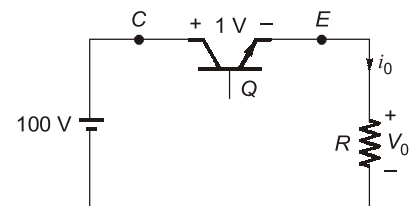
$$t_{\text{ON}} = t_{\text{OFF}} = 5 \mu\text{sec}$$

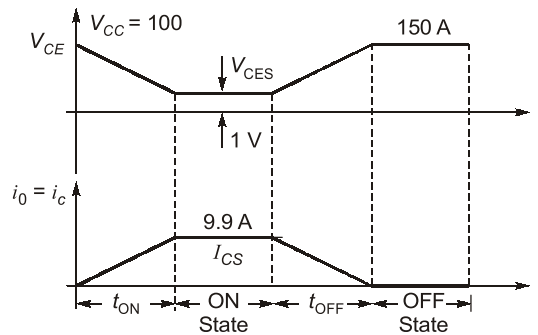
BJT \rightarrow ON (Ideal),

$$i_o = \frac{V_o}{R} = \frac{V_s}{R} = \frac{100}{10} = 10 \text{ A}$$

Considering V-drop :

$$i_o = \frac{V_s - V_{\text{drop}}}{R} = \frac{100 - 1}{10} = \frac{99}{10} = 9.9 \text{ A}$$





t_{ON} process :

$$i_C = \frac{I_{CS}}{t_{ON}} \cdot t ; \quad V_{CE} = -\left(\frac{V_{CC} - V_{CES}}{t_{ON}}\right)t + V_{CC}$$

Average power loss during t_{ON} process

$$= \frac{1}{T} \int_0^{t_{ON}} V_{CE} \cdot i_C \cdot dt = \frac{1}{T} \int_0^{t_{ON}} \left[-\left(\frac{V_{CC} - V_{CES}}{t_{ON}}\right)t + V_{CC} \right] \cdot \left(\frac{I_{CS}}{t_{ON}}\right) \cdot t \cdot dt$$

$$= f \cdot I_{CS} \cdot t_{ON} \left[\frac{V_{CC}}{2} - \frac{V_{CC} - V_{CES}}{3} \right] = 10 \times 10^3 \times 9.9 \times 5 \times 10^{-6} \left[\frac{100}{2} - \frac{100 - 1}{3} \right] = 8.415 \text{ W}$$

t_{OFF} process : Average power loss during t_{OFF} process

$$= \frac{1}{T} \int_0^{t_{OFF}} V_{CE} \cdot i_C \cdot dt = \frac{1}{T} \int_0^{t_{OFF}} \left[\left(\frac{V_{CC} - V_{CES}}{t_{OFF}}\right) \cdot t + V_{CES} \right] \cdot \left[\frac{-I_{CS}}{t_{OFF}} \cdot t + I_{CS} \right] \cdot dt \simeq f \cdot t_{OFF} \cdot \frac{I_{CS}}{6} (V_{CC} - V_{CES})$$

$$= 10 \times 10^3 \times 5 \times 10^{-6} \times \frac{9.9}{6} (100 - 1) = 8.1675 \text{ W}$$

On State : $V_{CE} = 1 \text{ V}, i_C = 9.9 \text{ A}$

Duty ratio : $\alpha = \frac{T_{ON}}{T} = T_{ON} \cdot f$

$$\therefore T_{ON} = \frac{\alpha}{f} = \frac{0.4}{10 \cdot 10^3} = 40 \mu\text{s}$$

\therefore Average power loss during ON state

P_{Avg} (On state) :

$$P_{Avg} \text{ (On State)} = \frac{1}{T} \int_0^{T_{ON}} V_{CE} \cdot i_C \cdot dt = f \int_0^{T_{ON}} 1 \times 9.9 \times dt = f \cdot T_{ON} \cdot 9.9 = 10 \times 10^3 \times 40 \times 10^{-6} \times 9.9 = 3.96 \text{ W}$$

$$P_{Avg} \text{ (OFF State)} = \frac{1}{T} \int_0^{T_{OFF}} V_{CE} \cdot i_C \cdot dt = 0$$

\therefore Total average power loss

$$= P_{Avg} (t_{ON} \text{ process}) + P_{Avg} \text{ (ON state)} + P_{Avg} (t_{OFF} \text{ process}) + P_{Avg} \text{ (OFF state)}$$

$$= 8.415 \text{ W} + 3.96 \text{ W} + 8.1675 + 0 = 20.54 \text{ W}$$

