ELECTRICAL ENGINEERING

POWER ELECTRONICS

Comprehensive Theory
with Solved Examples *and* Practice Questions

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Power Electronics

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CHAPTER

1

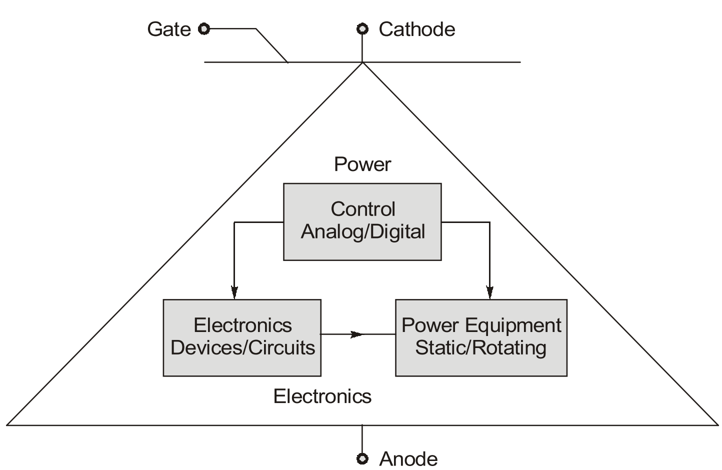
Introduction

1.1 POWER ELECTRONICS

Power electronics combines power, electronics and control. Controls deals with the steady-state and dynamic characteristics of closed-loop system. Power deals with static and rotating power equipment for the generation, transmission and distribution of electric energy. Electronics deal with the solid-state devices and grants for signal processing to meet the desired control objectives.

Power electronics may be defined as the application of solid-state electronics for the control and conversion of electric power. One could also define power electronics as the art of converting electrical energy from one form to another in an efficient, clean, compact and robust manner for the energy utilization to meet the desired needs.

The inter-relationship of power electronics with power, electronics and control is shown below in figure. The arrow points to the direction of the current flow from anode (A) to cathode (K). It can be turned on and off by a signal to the gate terminal (G). Without any gate signal, it normally remains in the off-state, behaves as an open circuit, and can withstand a voltage across the terminal A and K.



The task of power electronics is to process and control the flow of electric energy by supplying voltages and currents in a form that is optimally suited for user loads.

History of Power Electronics

The history of power electronics began with the introduction of the mercury arc rectifier in 1900. The first electronics revolution began in 1948 with the invention of the silicon transistor at Bell Telephone Laboratories by

CHAPTER

2

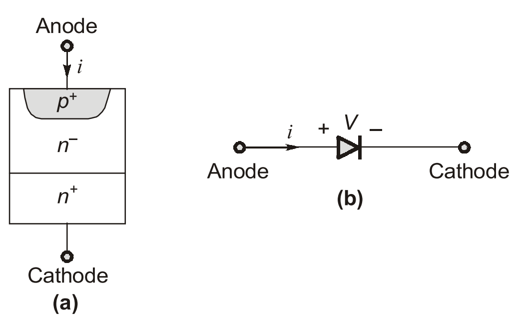
Power Semi-Conductor Diode and Transistor

2.1 BASIC SEMICONDUCTOR PHYSICS IMPORTANT CONCEPTS

- Current in a semiconductor is carried by both electrons and holes.
- Electron and holes move by both drift and diffusion.
- Intentional doping of the semiconductor with impurities will cause the density of holes and electrons to be vastly different.
- The density of minority carriers increases exponentially with temperature.
- A *pn* junction can be formed by doping one region *n*-type and the adjacent region *p*-type.
- A potential barrier is set up across a pn junction in thermal equilibrium that balances out the drift and diffusion of carriers across the junction so that no net current flows.
- In reverse bias a depletion region forms on both sides of the *pn* junction and only a small current can flow by drift.
- In forward bias large numbers of electrons and holes are injected across the *pn* junction and large currents flow by diffusion with small applied voltages.
- Large numbers of excess electron-hole pairs are created by impact ionization if the electric field in the semiconductor exceeds a critical value.
- Avalanche breakdown occurs when the reverse-bias voltage is large enough to generate the critical electric field E_{BD}.

2.2 BASIC STRUCTURE AND I-V CHARACTERISTICS

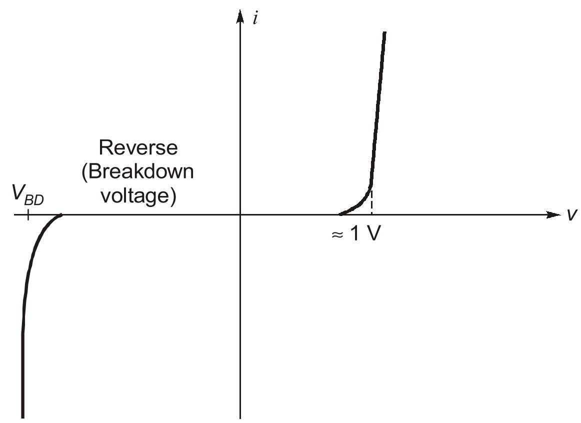
The practical realization of diode for power application is shown below :



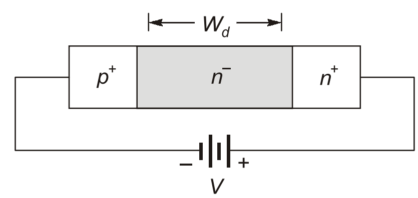
It consists of a heavily doped *n*-type substrate on top which is grown a lightly doped 'n^-' epitaxial layer of specified thickness. Finally, the *p-n* junction is formed by diffusing in a heavily doped *p*-type region that forms the anode of the diode.

The n^- layer which is often termed the drift region, is the prime structural feature not formed in low power diodes. Its function is to absorb the depletion layer of the reverse biased $p^+ \; n^-$ junction.

This relatively long lightly doped region would appear to add significant ohmic resistance to the diode when it is forward biased.



The current grows linearly with the forward bias voltage rather than exponentially.

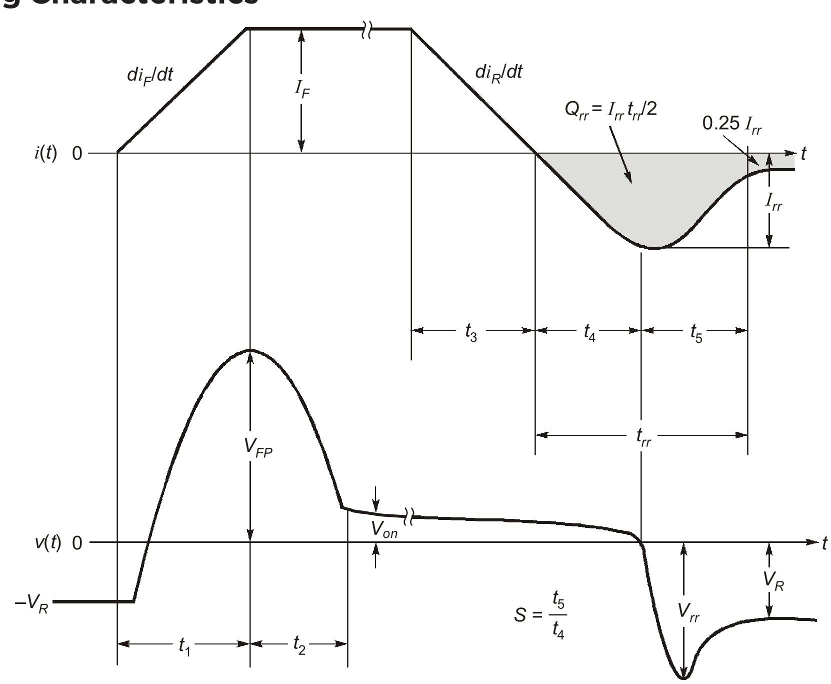


In reverse bias only a small leakage current, which is independent of the reverse voltage, flows until the reverse break down voltage V_{BD} is reached. When breakdown is reached the voltage appears to remain essentially constant while the current increases dramatically.

If the length W_d of the lightly doped region is longer than the depletion layer width at breakdown, then the structure is termed a non punch through diode, that is, the depletion layer has not reached through (or punched through) the lightly doped drift region and reached the highly doped n^+ subtract.

Two basic facts; first, large breakdown voltages require lightly doped junctions, at least on one side. Second, the drift layer in the diode must be fairly long in high voltage devices to accommodate the long depletion layers.

2.2.1 Switching Characteristics



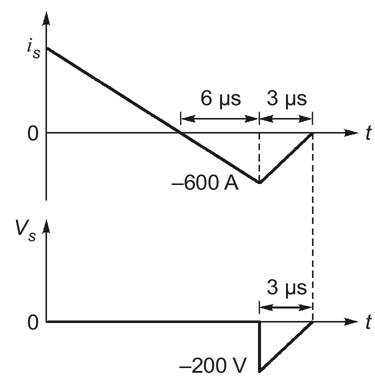
(a) 1 and 2 only
(b) 1, 2 and 3 only
(c) 2, 3 and 5 only
(d) 1, 2, 3, 4 and 5

Solution : (a)

SCR, GTO and TRIAC belong to the family of thyristors, while BJT, MOSFET and IGBT belong to the family of transistors.

OBJECTIVE BRAIN TEASERS

Q.1 During turn off a thyristor, idealized voltage and current waveforms are shown below. For a triggering frequency of 50 Hz, the mean power loss due to turn off is ______ W.



1. (6)

The power loss, $P = \frac{1}{T}\int_0^3 V_s(t)\, i_s(t)\, dt = \frac{1}{T}\int_0^3 \left(\frac{200}{3}t\right)\left(\frac{600}{3}t\right) dt = \frac{40000}{3T}\int_0^3 t^2\, dt = \frac{40000}{3T}\left[\frac{t^3}{3}\right]_0^3$

where T is in μsec $\Rightarrow$ $T = \frac{1}{50}\times 10^6 = 20000$

So, $P = \frac{40000}{3\times 20000}\left[\frac{3^3}{3}\right] = 6$ Watt average power loss

CONVENTIONAL BRAIN TEASERS

Q.1 A sinusoidal voltage source of $v(t) = 100\cos(377t)$ V is applied to a non-linear load, resulting in a non-sinusoidal current which is expressed in Fourier series form as

$$i(t) = 8 + 15\cos(377t + 30°) + 6\cos[2(377)t + 45°] + 2\cos[3(377)t + 60°]$$

Determine (a) the power absorbed by the load, (b) the power factor of the load, (c) the distortion factor of the load current, (d) the total harmonic distortion of the load current.

1. (Sol)

(a) The power absorbed by the load is determined by computing the power absorbed at each frequency in the fourier series.

$$P = (0)(8) + \left(\frac{100}{\sqrt{2}}\right)\left(\frac{15}{\sqrt{2}}\right)\cos 30° + 0\left(\frac{6}{\sqrt{2}}\right)\cos 45° + (0)\left(\frac{2}{\sqrt{2}}\right)\cos 60° = \left(\frac{100}{\sqrt{2}}\right)\left(\frac{15}{\sqrt{2}}\right)\cos 30° = 650 \text{ W}$$

(b) The rms voltage is : $V_{rms} = \dfrac{100}{\sqrt{2}} = 70.7$ V

and the rms current is computed : $I_{rms} = \sqrt{8^2 + \left(\frac{15}{\sqrt{2}}\right)^2 + \left(\frac{6}{\sqrt{2}}\right)^2 + \left(\frac{2}{\sqrt{2}}\right)^2} = 14.0$ A

The power factor is : $\text{pf} = \dfrac{P}{S} = \dfrac{P}{V_{rms}I_{rms}} = \dfrac{650}{(70.7)(14.0)} = 0.66$

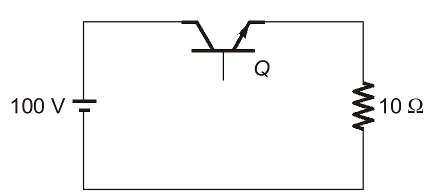
Alternatively, power factor can be computed : $\text{pf} = \dfrac{I_{1,rms}\cos(\theta_1 + -\phi_1)}{I_{rms}} = \dfrac{\left(\frac{15}{\sqrt{2}}\right)\cos(0-30°)}{14.0} = 0.66$

(c) The distortion factor is computed as : $\text{DF} = \dfrac{I_{1,rms}}{I_{rms}} = \dfrac{\frac{15}{\sqrt{2}}}{14.0} = 0.76$

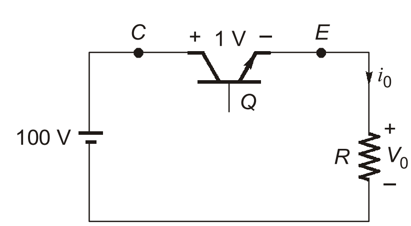
(d) The total harmonic distortion of the load current is obtained as

$$\text{THD} = \sqrt{\frac{I_{rms}^2 - I_{1,rms}^2}{I_{1,rms}^2}} = \sqrt{\frac{14^2 - \left(\frac{15}{\sqrt{2}}\right)^2}{\left(\frac{15}{\sqrt{2}}\right)^2}} = 0.86 = 86\%$$

Q.2 In the figure below, the transistor Q is operating at 10 kHz and 40% duty ratio. If the transistor has on-state voltage drop of 1 V and $t_{on} = t_{off} = 5$ μs, find its total losses during the operation.
(Assume linear rise and fall characteristics of the voltage and currents in the device during switching).



2. (Sol)



$t_{ON} = t_{OFF} = 5$ μsec

BJT → ON (Ideal),

$$i_o = \frac{V_o}{R} = \frac{V_s}{R} = \frac{100}{10} = 10 \text{ A}$$

Considering V-drop :

$$i_o = \frac{V_s - V_{drop}}{R} = \frac{100-1}{10} = \frac{99}{10} = 9.9 \text{ A}$$