ELECTRICAL ENGINEERING

Microprocessors

Comprehensive Theory
with Solved Examples *and* Practice Questions

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CONTENTS

Microprocessors

CHAPTER

1

Introduction to 8085 and Its Functional Organization

1.1 INTRODUCTION

The most important technological invention of modern times is the "microprocessor". A microprocessor is a multiple purpose programmable clock driven, register based electronic device that reads binary instructions from memory, accepts binary data as input and processing this data according to the instructions written in the memory.

The Figure shows the basic block diagram of a microcomputer which processes binary data and traditionally represented by four blocks i.e. CPU, memory, input device and output device.

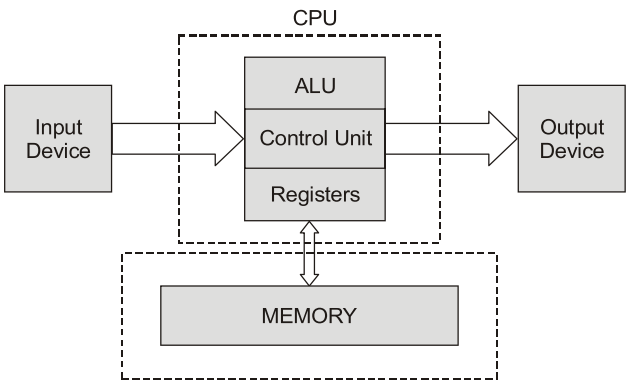


***Fig.:** Block diagram of microcomputer*

Here, input device is a device that transfers information from outside world to the computer for example: Key board, mouse, webcam, microphone, scanner, electronic white boards, etc. The output device transfers information from computer to the outside world like monitor, printers (all types), speakers, headphones, projector, plotter, Braille embosser, LCD projection panel, computer output microfilm (COM) etc. Memory is an electronic medium that stores binary information.

Central Processing Unit (CPU) is the heart of computer systems. The microprocessors in any microcomputer act as a CPU. The CPU can be made up with ALU + CU + Registers, where ALU is the group of circuits that perform arithmetic and logical operations. Control Unit (CU) is a group of circuits that provide timings and signals to all the operations in the computer and controls the data flow.

1.2 HISTORY OF MICROPROCESSORS

A brief review of certain microprocessors were given in the Table. Intel introduced its first 4-bit PMOS microprocessor 4004 in the year 1971. It has 16 pins, 640-bytes of memory addressing capability and 10 address lines. After this enhanced version of 4004, a 4-bit, Intel 4040 was developed. In 1972, Intel introduced its first 8-bit processor Intel 8008, which also uses PMOS technology. The PMOS technology processors were slow and not compatible with TTL logic. These microprocessors could not survive as general purpose microprocessor due

to design limitations. In 1974, Intel introduced its more powerful and faster 8 bit NMOS microprocessor Intel 8080. These processors were faster and compatible with TTL logic. Intel 8085 followed 8080 microprocessor. The main limitations of 8 bit microprocessors tempted the designers to go for more powerful processors in terms of advanced architecture, more processing capability, larger memory addressing capability and more powerful instruction set. The Intel 8086 was the result, launched in 1978 . The technology used was HMOS, high speed and high performance MOS technology.

Most of the general purpose microprocessors used in the modern world computers are the family of 8086.

Microprocessor	Word length	Memory capacity
Intel 4004 (PMOS)	4-bit	640 B
Intel 8008	8-bit	16 kB
Intel 8080 (NMOS)	8-bit	64 kB
Intel 8085 (NMOS)	8-bit	64 kB
Intel 8086 (HMOS)	16-bit	1 MB
Intel 8088	8/16-bit	1 MB
Intel 80186	16-bit	1 MB
Intel 80286	16-bit	16 MB real, 4 GB virtual
Intel 80386	32-bit	4 GB real, 4 GB virtual
Intel 80486	32-bit	4 GB real, 64 TB virtual
Pentium-II	64-bit	64 GB real
Z-80	8-bit	64 kB
Z-800	8-bit	500 kB

Table: *A brief review of various microprocessors*

1.3 COMPUTER LANGUAGE

- **Scale of integration:**
  - **SSI (Small Scale Integration):** The term refers to the technology used to fabricate discrete logic gates on a chip.
  - **MSI (Medium Scale Integration):** The process of designing few tens of gates on a single chip.
  - **LSI (Large Scale Integration):** The process of designing hundreds of gates on a single chip similarly terms VLSI (very large scale integration), ULSI (ultra large scale integration) are used to indicate the scale of integration.
- **Digital computer:** A programmable machine that processes binary data. It is traditionally represented by five components: CPU, ALU, CU, memory, input and output.
- **Instruction:** a command in binary that is recognized and executed by the computer in order to accomplish a task. Some instructions are designed with one word, and some require multiple words.
- **Mnemonic:** a combination of letters to suggest the operation of an instruction.
- **Program:** a set of instructions written in a specific sequence for the computer to accomplish a given task.
- **Machine Language:** the binary medium of communication with a computer through a designed set of instructions specific to each computer.
- **Assembly Language:** a medium of communication with a computer in which programs are written in mnemonics. An assembly language is specific to a given computer.
- **Low-Level Language:** a medium of communication that is machine-dependent or specific to a given computer. The machine and the assembly languages of a computer are considered low-level languages. Programs written in these languages are not transferrable to different types of machines.
- **High-Level Language:** a medium of communication that is independent of a given computer. Programs are written in English-like words, and they can be executed on a machine using a written translator (a compiler or an interpreter).
- **Compiler:** a program that translates English-like words of a high-level language into the machine language of a computer. A compiler reads a given program, called a source code, in its entirety, and then translates the program into the machine language which is called an object code. (Ex. *C*, *C++*)

EXAMPLE : 1.16

Which of these is software interrupt?

(a) RST 4.5 (b) RST 5 (c) RST 5.5 (d) RST 6.5

Solution : (b)

Except RST 5 all other options are the example of hardware interrupts.

Trick for finding vectors address:

Firstly we get (n × 8), where n = 0,1,2, ...7. Then after convert it in hexadecimal.

e.g.:**RST 2**, n = 2 ∴ n × 8 = 16 $\xrightarrow{\text{Hexa}}$ $(0010)_H$

EXAMPLE : 1.17

What is the vectored address of interrupt RST5?

(a) 0040 H (b) 0028 H (c) 0005 H (d) 0008 H

Solution : (b)

Vectored address for RST n = $n \times 8$

Here, $n = 5$

$5 \times 8 = (40)_{10} = (28)_{16} \Rightarrow 0028\,H$

SUMMARY

- The 8085 microprocessor (μP) is an improved version of 8080 A.
- 8085 μP has 74 instruction sets.
- The programming of 8085 μP is done in Assembly language.
- There are 27 pins (16 + 1 + 1 + 9) for output in a 8085 μP.
- There are 21 pins for input in a 8085 μP.
- In 8085 μP, memory it contains 2^{16} address line or 64 K or 65536 memory locations and each location can stores 8 bit. So, we can say the memory capacity of 8085 μP equals to 64 k × 8 bit ≈ 64 k bytes.
- A "TRISTATE DEVICE" has 3 states, two logic states (1 or 0) and one high impedance state.

  When device is disabled, it remains in high impedance state and doesn't draw any current from the system.
- To interconnect peripherals with the microprocessor, additional logic circuitry (Buffers, Decoders, Encoders and Latches) are needed.
- Performance of "Cache Memory" are measured in "Hit ratio".
- An I/O processor controls the flow of information between main memory and I/O devices.
- "Cache Memory" is a small high-speed memory placed between the CPU and the main memory (RAM).
- When a CPU is interrupted, it acknowledges interrupt and branches to a subroutine.
- The reference bit is used for the purpose of implementing NRU (Not recently used) algorithm.
- The larger the RAM of a computer, the faster is its speed, since it eliminates frequent disk I/Os.
- An "Assembler" is used for translation of a program from assembly language to Machine language.

OBJECTIVE BRAIN TEASERS

Q.1 In 8085 microprocessor unit scratch pad memory comprises of
(a) *B*, *C*, *D*, *E*, *H* and *L* Registers
(b) *W*, *Z*, *B*, *C*, *D*, *E*, *H* and *L* Registers
(c) *W*, *Z*, *B*, *C*, *D* and *E* Registers
(d) *W*, *Z*, *B*, *C*, *D*, *E*, *H*, *L* and status Registers

Q.2 An interrupt in which the external device supplies its address as well as the interrupt request is known as
(a) vectored interrupt
(b) maskable interrupt
(c) polled interrupt
(d) non-maskable interrupt

Q.3 **Assertion (A):** The data bus and address bus of 8085 microprocessor are multiplexed.
Reason (R): Multiplexing reduces number of pins.
(a) Both A and R are correct and R is correct explanation of A.
(b) Both A and R are correct but R is not correct explanation of A.
(c) Only A is correct.
(d) Only R is correct.

Q.4. **P :** Program counter is the register which stores the address of the next instruction to be executed.
Q : Stack pointer stores the address of the top of the stack.
Out of these two statements, which statement/s is/are true?
(a) Only P (b) Only Q
(c) Both P and Q (d) None of them

Q.5 How many instructions does microprocessor 8085 has?
(a) 255 (b) 256
(c) 246 (d) 250

Q.6 How many nibbles are there in 1 kbyte data?
(a) 500 (b) 1024
(c) 2048 (d) none of these

Q.7 Match **List-I (Interrupt)** with **List-II (Property):**

List-I		List-II
P.	RST 7.5	1. Non-maskable
Q.	RST 6.5	2. Edge sensitive
R.	INTR	3. Level sensitive
S.	TRAP	4. Non-vectored

Codes:

	P	Q	R	S
(a)	1	3	4	2
(b)	2	4	3	1
(c)	1	4	3	2
(d)	2	3	4	1

Q.8 For fetch machine cycle the status signal S_1 and S_0 are respectively
(a) 0 and 0 (b) 0 and 1
(c) 1 and 0 (d) 1 and 1

Q.9 In INTEL 8085, while executing a program non maskable interrupt occurs. The data present on data line is
(a) 00 H (b) 24 H
(c) 36 H (d) can't be predicted

Q.10 Consider the table given below.

IO/$\overline{M}$	S_1	S_0	Machine cycle
0	1	1	*X*
1	0	1	*Y*
1	1	1	*Z*

Here S_0, S_1 are status signals.
X, *Y*, *Z* are respectively.
(a) Interrupt acknowledgment, I/O read, opcode fetch.
(b) Interrupt acknowledgment, I/O write, opcode fetch.
(c) Opcode fetch, I/O read, Interrupt acknowledgment.
(d) Opcode fetch, I/O write, Interrupt acknowledgment.

ANSWERS KEY

1. (a)	**2.** (c)	**3.** (a)	**4.** (c)	**5.** (c)
6. (c)	**7.** (d)	**8.** (d)	**9.** (b)	**10.** (d)

HINTS & EXPLANATIONS

1. (a)

W and *Z* register are temporary register and does not belong to scratch pad registers.

6. (c)

No. of bits in a nibble = 4 bits

Total no. of bits in 1 kB data is

$= 1 \times 2^{10} \times 8$ bits

$= 2^{13}$ bits

$\therefore$ No. of nibbles $= \dfrac{2^{13}}{4} = 2^{11} = 2048$

7. (d)

INTR is a non vectored interrupt.

TRAP is a Non-Maskable interrupt.

RST 7.5 is Edge sensitive interrupt.

8. (d)

S_1	S_0	Operation
0	0	Halt
0	1	Write operation
1	0	Read operation
1	1	Opcode fetch

9. (b)

TRAP is a non-maskable interrupt in 8085 μP.

TRAP [RST 4.5]

Vectored Address $= 4.5 \times 8 = (36.0)_{10}$

$= (36)_{10} = (24)_{16} = 24$ H

10. (d)

$IO/\overline{M}$	S_1	S_0	Machine Cycle
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O Write
1	1	1	Interrupt acknowledge
X	0	0	Halt

$\therefore$ $X \rightarrow$ Opcode fetch

$Y \rightarrow$ IO write

$Z \rightarrow$ Interrupt acknowledgement

CONVENTIONAL BRAIN TEASERS

Q.1 The number of flip-flops in a flag register of INTEL 8085 are _____.

1. (Sol.)

Number of flip-flops in flag register of INTEL 8085 are 5 to 8.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	X	AC	X	P	X	CY

Flag Register

Best possible answer is 5.

Flag register is an 8 bit register having five 1-bit flip-flops, which holds either 0 or 1 depending upon the result stored in the accumulator.

Q.2 Maximum memory that can be connected to INTEL 8085 is _____ bytes.

2. (Sol.)

Maximum memory that can be connected to INTEL 8085 in 2^n, where n is address lines. INTEL 8085 have 16 address lines.

$\therefore$ Maximum memory $= 2^{16} = 65536$

Q.3 Explain the difference between a compiler and an interpreter.

3. (Sol.)

Basis of Comparision	Assembler	Compiler
Conversion	Assembler converts the assembly code into the machine code.	Compiler converts the source code written by the programmer to a machine level language.
Input	Assembler inputs source code.	Compiler inputs is preprocessed source code.
The output	The output of assembler is binary code	The output of compiler is a mnemonic version of machine code.
Examples	GAS GNU	C C # Java C++
Debugging	Debugging is difficult.	Debugging is easy.
Working	Assembler converts source code to an object code first then it converts the object code to the machine language with the help of linker programs.	Compiler scans the entire program first before translating into machine code.
Intelligence	Assembler is less intelligent than a compiler.	Compiler is more intelligent than assembler.
Working Phases	Assembler makes works in two phases over the given input. The phases are: First Phase Second Phase	The compilation phases are: Lexical analyzer Syntax analyzer Semantic analyzer Code optimizer Code generator Error handler

Q.4 Explain the functions of the ALE and IO/$\overline{M}$ signals of the 8085 μP.

4. (Sol.)

ALE (Address Latch Enable): It is a special signal used to demultiplex the address bus and data bus. This is a positive going pulse generated every time the processor begins an operation (machine cycle) to latch the low-order address from the multiplexed bus and generate a separate set of eight address lines A_7 to A_0.

ALE = 1 $\Rightarrow$ Address transfer to bus (A_7 to A_0 lines are activated as address bus)

ALE = 0 $\Rightarrow$ Data transfer to bus (A_7 to A_0 lines are activated as data bus)

$IO/\overline{M}$: This is the status signal used to differentiate betweeen I/O and memory operations.

$IO/\overline{M} = 1 \Rightarrow$ An IO operation performed (Address on the address bus is for input output devices)

$IO/\overline{M} = 0 \Rightarrow$ A memory operation performed (Address on the address bus is for the memory)

■■■■

CHAPTER

2

Microprocessor Interfacing

2.1 INTRODUCTION

In a microprocessor based system the designer has to select suitable memories and I/O devices for performing his task and so they interface them to the microprocessor. Several memory chips and I/O devices are connected to a microprocessor. Figure (a) shows the schematic diagram to interface memory chips and I/O devices to a microprocessor.

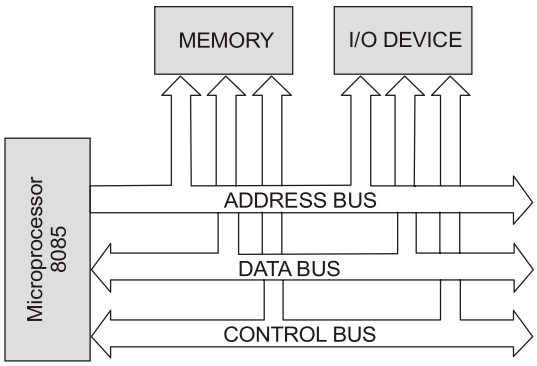


Fig.: (a)

An address decoding circuit is employed to select the required I/O device of a memory chip. Figure (b) shows the schematic of a decoder circuit.

If IO/$\overline{M}$ is high; decoder 2 is activated and the required I/O device is selected.

If IO/$\overline{M}$ is low, decoder 1 is activated and the required memory is selected.

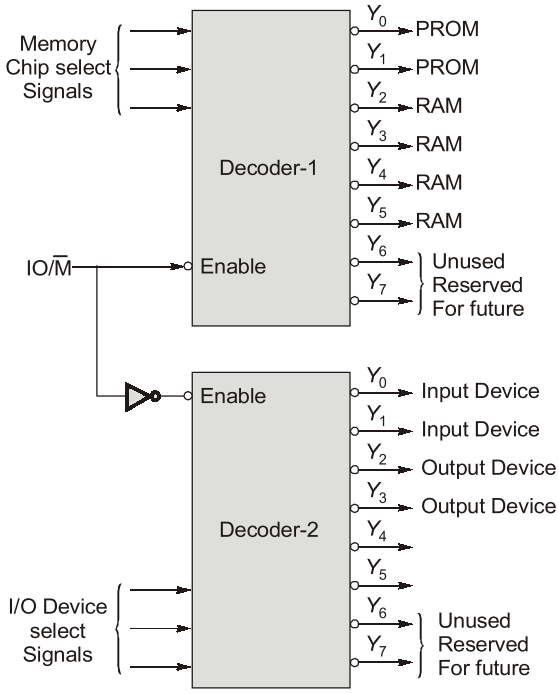


Fig.: (b)

2.2 MEMORY INTERFACING

During the execution of a program the microprocessor needs to access memory quite frequently to read the instruction codes and enable that access. The primary function of memory interfacing is that the microprocessor

should be able to read from and write into a given register of memory chip. To perform these operations, the microprocessor should be able to

1. Select chip
2. Identify the register
3. Enable the appropriate buffer

A memory chip select decoder is used to provide chip select signal for each memory device. This will decide the address range that is allotted for each memory IC. The decoding task can be performed by a decoder, a comparator, a bipolar PROM or PLA.

The application of 74LS138, a 3 to 8 time decoder is illustrated in Figure. Here G_1, $\overline{G_2A}$ and $\overline{G_2B}$ are enable signals. G_1 is an active high signal where as $\overline{G_2A}$ and $\overline{G_2B}$ are active low signals. Thus, to enable the decoder G_1 should be high and $\overline{G_2A}$ and $\overline{G_2B}$ should be low. A, B and C are the select lines and Y_0 to Y_7 are output lines. By applying the proper logic to these lines any one of the outputs can be selected.

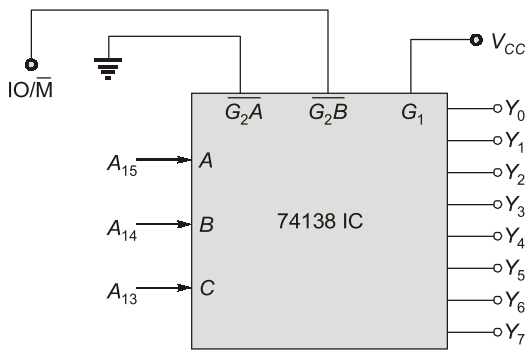


***Fig.:** Interfacing of memory device using 74LS138*

The Intel 8085 uses 16-bit address bus for addressing memory chips and I/O devices, thus can access 2^{16} = 64 kB memory and I/O devices. The entire memory address has been divided in to 8 zones (0000 H to FFFF H). Address lines A_{15}, A_{14} and A_{13} have been applied to the select line A, B and C of 74LS138. The logic applied to these lines selects a particular memory device (EPROM or RAM). Rest of the address lines ($A_{12} - A_0$) directly connected to the memory chip thus decide the address of memory location. IO/$\overline{M}$ is connected to $\overline{G_2B}$, it goes low for memory read/write operations. G_1 is connected to V_{CC} and $\overline{G_2A}$ is grounded.

Interfacing of ROM with 8085 Microprocessor (MPU)

- The chip is first enabled by sending a low (0) to $\overline{CS}$ input of ROM. The required address is sent on the address bus by the MPU.
- The built in decoder of ROM connects to the required 12 bit address. A short time later a low (0) on the Read line enables the output ($\overline{OE}$) of the ROM. Stored data is placed on the data bus and fed to the MPU.

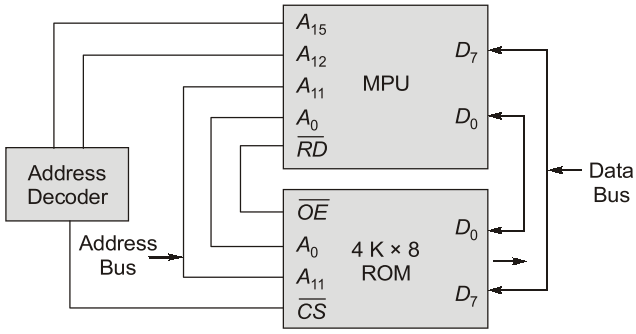


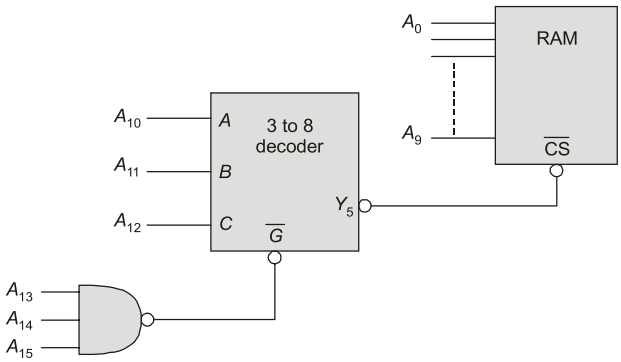
***Fig.:** Interfacing of ROM with MPU*

- In this one critical time limitation is the Read Access Time, i.e. the time it takes to locate the correct memory word (byte) after the chip is enabled, by the ROM's internal decoder.
- Thus while interfacing the MPU with the ROM, the important considerations are addressing and timing.
- Since a ROM can only be read, the data bus will be in the output mode only and the Read line only will be connected to it.

OBJECTIVE BRAIN TEASERS

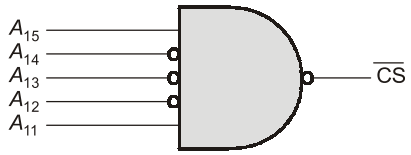
Q.1 Sixty-four number of 256 ×1 bit RAM IC is arranged in 8 rows and 8 columns to get memory
(a) 1 kB (b) 2 kB
(c) 4 kB (d) 8 kB

Q.2 The range of the addresses of the RAM which is interfaced to a microprocessor as shown in figure is



(a) 1400 H - 17FF H (b) E400 H - EFFF H
(c) F000 H - FFFF H (d) F400 H - F7FF H

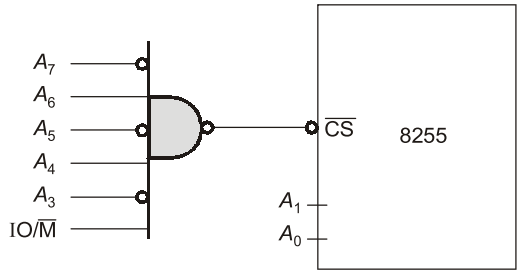
Q.3 The logic circuit given below is used to generate chip select signal by INTEL 8085 microprocessor to address a peripheral. The peripheral will respond to address in the range.



(a) 7800 H – 7FFF H (b) 9800 H – 9FFF H
(c) 8000 H – 7FFF H (d) 8800 H – 8FFF H

Q.4 For 16 bit address-bus, if an 8K RAM chip is selected when A_{13}, A_{14} and A_{15} address bits are all one, then what is the range of the memory address?
(a) E000H - EFFFH (b) E000H - FFFFH
(c) F000H - FFFFH (d) F000H - FEEEH

Q.5 An 8255 chip is interfaced with 8085 has I/O mapped I/O as shown in figure below. The address lines A_3 to A_7 as well as IO/$\overline{M}$ signals are used for address decoding. The address lines A_0 and A_1 are used by the 8255 chip to decode its 3 ports and control register internally. The range of addresses for which the 8255 chip would get selected is



(a) 50 – 53 H, 54 – 57 H
(b) A8 – AB H, AC – AF H
(c) 50 – AF H
(d) None of these

Q.6 If a page of memory is assumed to be 256 bytes then in how many pages total memory of 8085 can be treated ?
(a) 8 (b) 128
(c) 256 (d) 2048

ANSWERS KEY

1. (b) **2.** (d) **3.** (d) **4.** (b) **5.** (a)
6. (c)

HINTS & EXPLANATIONS

1. (b)

Size of RAM IC = 256 × 1
Total No. of RAM IC = 64
Hence total memory size = 64 × 256 × 1 bits
Given 8 column and 8 rows.
Total memory size
$= 2^6 \times 2^8 \times 1$
$= 2^3 \times 2^8 \times 8$
$= 2 \times 2^{10} \times 8$ bits
= 2 k × 8 bits
= 2 kB

2. (d)

To generate the address, the RAM chip should be selected.

Hence, the decoder should also be enabled.

$\overline{G}$ pin of decoder is active low pin.

Lower Address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
1	1	1	1	0	1	0	0
F				4			

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0
0				0			

Upper Address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
1	1	1	1	0	1	1	1
F				7			

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	1	1	1	1	1	1	1
F				F			

Hence, the address range is F400H – F7FFH

3. (d)

The peripheral will respond to address in range.

Lower Address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
1	0	0	0	1	0	0	0
8				8			

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0
0				0			

Upper Address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
1	0	0	0	1	1	1	1
8				F			

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	1	1	1	1	1	1	1
F				F			

∴ Address Range 8800 H – 8FFFH

4. (b)

16 bit address bus.

8K RAM chip = $2^3 \times 2^{10} = 2^{13}$

Hence, the address lines of RAM chip are 13.

A_{13}, A_{14}, A_{15} lines are used for chip select when all are 1.

Lower Address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
1	1	1	0	0	0	0	0
E				0			

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0
0				0			

Upper Address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
1	1	1	1	1	1	1	1
8				F			

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	1	1	1	1	1	1	1
F				F			

Address Range ⇒ E000 H – FFFFH

5. (a)

The address range for which 8255 chip would get selected is given as

Case (1): Taking A_2 as '0'.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	1	0	1	0	0	0	0	→ Port A
0	1	0	1	0	0	0	1	→ Port B
0	1	0	1	0	0	1	0	→ Port C
0	1	0	1	0	0	1	1	→ CW Reg

Hence the address range 50 – 53 H

Case (2): Taking A_2 as '0'.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	1	0	1	0	1	0	0	→ Port A
0	1	0	1	0	1	0	1	→ Port B
0	1	0	1	0	1	1	0	→ Port C
0	1	0	1	0	1	1	1	→ CW Reg

∴ Address range ⇒ 54 – 57 H

6. (c)

Total memory of 8085 is $2^{16} \times 8$ bits

Size of page of memory is 256 bytes

$= 256 \times 8$ bits

$$\therefore \text{No. of pages} = \frac{2^{16} \times 8}{256 \times 8} = 256 = 2^8$$

Hence, 256 pages are required for total memory of 8085.