MADE EASY PUBLICATIONS

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CONTENTS

ELECTRICAL ENGINEERING

Objective Practice Sets

Computer Fundamentals

1 CHAPTER
Memory Organization and IO Organization

Q.1 More than one word are put in one cache block to
(a) Exploit the temporal locality of reference in a program.
(b) Exploit the spatial locality of reference in a program.
(c) Reduce the miss penalty.
(d) None of the above

Q.2 The access time of a word in a 4 MB main memory is 100 ns. The access time of a word in a 32 kB data cache memory is 10 ns. The average data cache hit ratio is 0.95. The effective memory access time is
(a) 9.5 ns (b) 15 ns
(c) 20 ns (d) 50 ns

Q.3 A memory system of size 128 K bits is required to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is
(a) 64 (b) 4
(c) 8 (d) 16

Q.4 The main memory of a computer has 2 cm blocks while the cache has 2 c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set
(a) (k mod m) of the cache
(b) (k mod c) of the cache
(c) (k mod 2 c) of the cache
(d) (k mod 2 cm) of the cache

Q.5 When an interrupt occurs, an operating system
(a) ignores the interrupt
(b) always changes state of interrupted process after processing the interrupt
(c) always resumes execution of interrupted process after processing the interrupt
(d) may change state of interrupted process to 'blocked' and schedule another process

Q.6 A system uses FIFO policy for page replacement. It has 4 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur?
(a) 196 (b) 192
(c) 197 (d) 195

Q.7 If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?
(a) Width of tag comparator
(b) Width of set index decoder
(c) Width of way selection multiplexor
(d) Width of processor to main memory data bus

Q.8 According to temporal locality, processes are likely to reference pages that
(a) have been referenced recently.
(b) are located at address near recently referenced pages in memory.
(c) have been preloaded in memory.
(d) None of these

Q.9 The principle of locality justifies the use of
(a) Interrupts (b) Threads
(c) DMA (d) Cache Memory

Q.10 Consider a system with 2 level cache. Access times of level 1 cache, level 2 cache and main memory are 1 ns, 10 ns and 500 ns respectively. The hit rates of level 1 and level 2 caches are 0.8 and 0.9 respectively. What is the average access time of the system ignoring the search time within the cache?
(a) 13.0 (b) 12.8
(c) 12.6 (d) 12.4

Q.11 A disc drive has an average seek time of 10 ms, 32 sectors on each track and 512 bytes per sector. If the average time to read 8 kbytes of

continuously stored data is 20 ms, what is the rotational speed of the disc drive?
(a) 3600 rpm (b) 6000 rpm
(c) 3000 rpm (d) 2400 rpm

Q.12 The access time of a cache memory is 100 ns and that of main memory is 1 µs. 80% of the memory requests are for read and others are for write. Hit ratio for read only accesses is 0.9. A write through procedure is used. The average access time of the system for both read and write requests is
(a) 200 ns (b) 360 ns
(c) 720 ns (d) 1100 ns

Q.13 A computer system has a 4 K word cache organized in block-set associative manner with 4 blocks per set, 64 words per block. The numbers of bits in the SET and WORD fields of the main memory address formula are respectively
(a) 15 and 4 (b) 6 and 4
(c) 7 and 2 (d) 4 and 6

Q.14 Which of the following requires a device driver?
(a) Register (b) Cache
(c) Main memory (d) Disk

Q.15 Which of the following semiconductor memory is used for cache memory?
(a) SRAM (b) DRAM
(c) ROM (d) PROM

Q.16 In a cache with 64-byte cache lines, how many bits are used to determine which byte within a cache line an address points to?
(a) 16 (b) 8
(c) 6 (d) 3

Q.17 Consider a system that uses interrupt driven I/O for a particular device which has an average data transfer rate of 8 kbps. The processing of the interrupt which includes the time to jump to ISR, its execution and returning to the main program is 100 µs. What fraction of processor time consume by the device, if the device interrupts for every 1 byte (in %)?
(a) 80 (b) 40
(c) 20 (d) 100

Q.18 The write through procedure is used
(a) To write on the memory directly.
(b) To write and read from memory simultaneously.
(c) To write directly on the memory and cache whenever a hit occurs on a cache.
(d) None of the above.

Q.19 The fastest data access is provided using
(a) Caches (b) DRAM's
(c) SRAM's (d) Registers

Q.20 The minimum time delay between the initiations of two independent memory operations is called
(a) Access Time (b) Cycle Time
(c) Transfer Time (d) Latency Time

Q.21 A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?
(a) 10 (b) 6.4
(c) 1 (d) 0.64

Q.22 A cache contains n blocks and main memory contains m blocks. If k-way set associative mapping is used then what will be number of TAG bits.
(a) $\log_2 \frac{mk}{n}$ (b) $\log_2 \frac{m}{n}$
(c) $\log_2 \frac{nk}{m}$ (d) $\log_2 \frac{mn}{k}$

Q.23 Which of the following statements are true?
1. Update bit is used in the write back cache to indicate the cache updation.
2. In hierarchical memory access organization CPU perform read and write operation on only level 1 memory.
3. In simultaneous memory access organization CPU perform read and write operation on any level of memory.

(a) 1 and 2 only (b) 1 and 3 only
(c) 2 and 3 only (d) 1, 2 and 3 only

Q.24 Which of the following is true?
(a) In write through protocol, cache location and main memory location are updated simultaneously.
(b) In write back protocol, cache location and main memory location are updated simultaneously.
(c) Modified or dirty bits are used by write through protocol.
(d) None of these

Q.25 In a vectored interrupt :
(a) the interrupting device supplies the branch information to the processor through an interrupt vector.
(b) the CPU does not know, which device cause the interrupt without polling each I/O interface.