ELECTRICAL ENGINEERING

COMPUTER FUNDAMENTALS

Comprehensive Theory
with Solved Examples *and* Practice Questions

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Computer Fundamentals

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Computer Fundamentals

Goal of the Subject

Basic understanding of Computer Fundamentals includes, the study about the basic architecture of computer, its Central Processing Unit (CPU), how the memory organization is done, I/O organization, data representation, basics of operating systems, file systems, basics of networking and elements of programming languages.

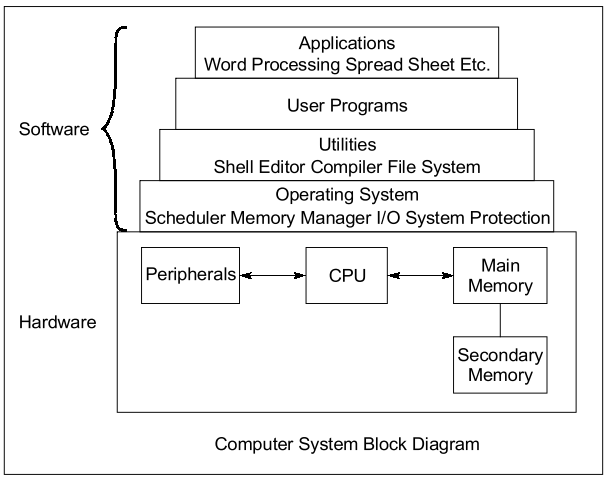
CHAPTER

1

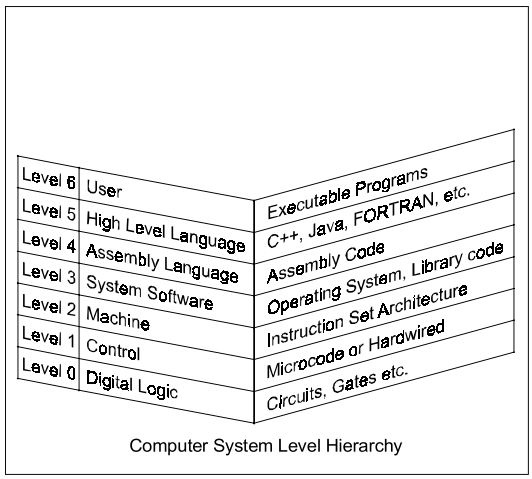
Basic Architecture

1.1 Computer System

Computer system is divided into two functional entities: Hardware and Software.



Computer System Block Diagram



Computer System Level Hierarchy

- **Hardware:** Lowest level in a computer are all the electronic circuits and physical devices from which it is built.

  Hardware consisting of its physical devices (CPU, memory, bus, storage devices, ...)
- **Software:** Sequences of instructions and data that make computers do useful work.

  Software, consisting of the programs it has (Operating system, applications, utilities, ...)

  Program is a sequence of instructions for a particular task.
- Operating system is set of programs included in system software package and Link between hardware and user needs.

1.7.4 Issues of Computer Design

- Cannot assume infinite speed and memory.
- Speed mismatch between memory and processor
- Handle bugs and errors
- Multiple processors, processes, threads
- Shared memory
- Disk access
- Better performance with reduced power

Summary

- **Computer:** A device that accepts input, processes data, stores data, and produces output, all according to a series of stored instructions.
- **Hardware:** Includes the electronic and mechanical devices that process the data; refers to the computer as well as peripheral devices.
- **Software:** A computer program that tells the computer how to perform particular tasks.
- **Computer organization:** Interconnection of hardware to form the computer system
- **Computer architecture:** the structure and behaviour of the computer perceived by the user.
- **Input:** Whatever is put into a computer system.
- **Data:** Refers to the symbols that represent facts, objects, or ideas.
- **Information:** The results of the computer storing data as bits and bytes; the words, numbers, sounds, and graphics.
- **Output:** Consists of the processing results produced by a computer.
- **Main Memory:** Area of the computer that temporarily holds data waiting to be processed, stored, or output. *Example:* Cache and Main memory
- **Secondary Storage:** Area of the computer that holds data on a permanent basis when it is not immediately needed for processing. Example: Disk, Floppy, etc.

Student's Assignments

Q.1 A 32-bit address bus allows access to a memory of capacity
(a) 64 MB (b) 16 MB
(c) 1 GB (d) 4 GB

Q.2 The system bus is made up of
(a) data bus
(b) data bus and address bus
(c) data bus and control bus
(d) data bus, control bus and address bus

Q.3 Which of the following is not involved in a memory write operation?
(a) MAR (b) PC
(c) MDR (d) data bus

Q.4 The read/write line
(a) belongs to the data bus
(b) belongs to the control bus
(c) belongs to the address bus
(d) CPU bus

Q.5 _____ is a piece of hardware that executes a set of machine-language instructions.
(a) controller (b) bus
(c) processor (d) motherboard

Q.6 Given below are some statements associated with the registers of a CPU. Identify the false statement.

(a) The program counter holds the memory address of the instruction in execution.
(b) Only opcode is transferred to the control unit.
(c) An instruction in the instruction register consists of the opcode and the operand.
(d) The value of the program counter is incremented by 1 once its value has been read to the memory address register.

Q.7 The following are four statements regarding what a CPU with only a set of 32-bit registers can perform?
1. Hold and operate on 32-bit integers
2. Hold and operate on 16-bit integers
3. Hold and operate on 64-bit floating point arithmetic
4. Hold and operate on 16-bit UNICODE characters

Which of the following is true about such a CPU?
(a) all are true (b) 1,2 and 3 only
(c) 1,2 and 4 only (d) 1,3 and 4 only

Q.8 The following are four statements about Reduced Instruction Set Computer (RISC) architectures.
1. The typical RISC machine instruction set is small, and is usually a subset of a CISC instruction set.
2. No arithmetic or logical instruction can refer to the memory directly.
3. A comparatively large number of user registers are available.
4. Instructions can be easily decoded through hard-wired control units.

Which of the above statements is true?
(a) 1 and 3 only
(b) 1,3 and 4 only
(c) 1, 2 and 3 only
(d) All of these

Q.9 The word length of a CPU is defined as
(a) the maximum addressable memory size.
(b) the width of a CPU register (integer or float point).
(c) the width of the address bus.
(d) the number of general purpose CPU registers.

Q.10 Which of the following statements is false about CISC architectures?
(a) CISC machine instructions may include complex addressing modes, which require many clock cycles to carry out.
(b) CISC control units are typically micro-programmed, allowing the instruction set to be more flexible.
(c) In the CISC instruction set, all arithmetic/logic instructions must be register based.
(d) CISC architectures may perform better in network centric applications than RISC.

Q.11 Which one is required while establishing the communication link between CPU and peripherals?
(a) Synchronization mechanism
(b) Conversion of signal values
(c) Operating modes
(d) All of the above

Student's Assignments — Answer Key

1. (d)	**2.** (d)	**3.** (b)	**4.** (b)	**5.** (c)
6. (a)	**7.** (c)	**8.** (d)	**9.** (b)	**10.** (c)
11. (d)				

■■■■

CHAPTER

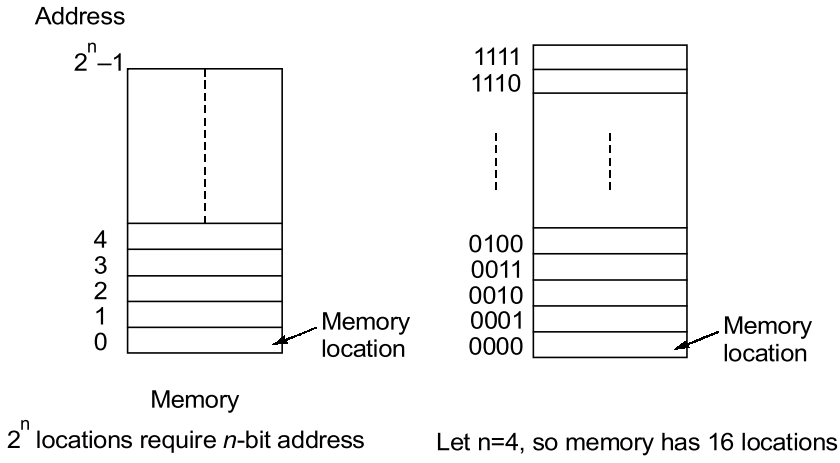
2

CPU Organization

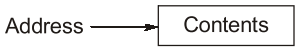
2.1 Introduction

How to address main memory?

Main memory is a set of storage locations. Each location of memory has a unique address (a binary number starting from zero). Each "addressable" location holds a fixed number of bits. Any location can be accessed at high speed in any order (random access memory).



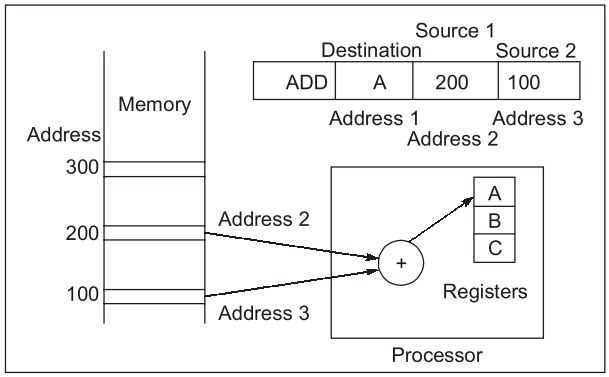
Memory consists of addressable locations. A memory location has 2 components: Address and Contents.



Data transfer between CPU and memory involves address bus and data bus

There are two ways stored information can be organized.

1. **Little Endian (little end first):** First location can hold least significant byte.
   Example: Intel uses little endian



Disadvantages of three address instructions:

- It has long instruction length.
- There may be three memory accesses needed for an instruction.

***Example* - 2.1** Write the three address instructions for the following statement.

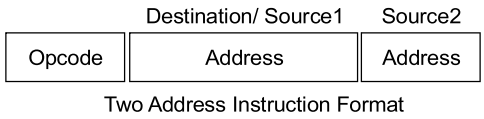
$$X = (A + B) \times (C + D)$$

Solution:

ADD R1, A, B	R1 ← M[A] + M[B]
ADD R2, C, D	R2 ← M[C] + M[D]
MUL X, R1, R2	M[X] ← R1 × R2

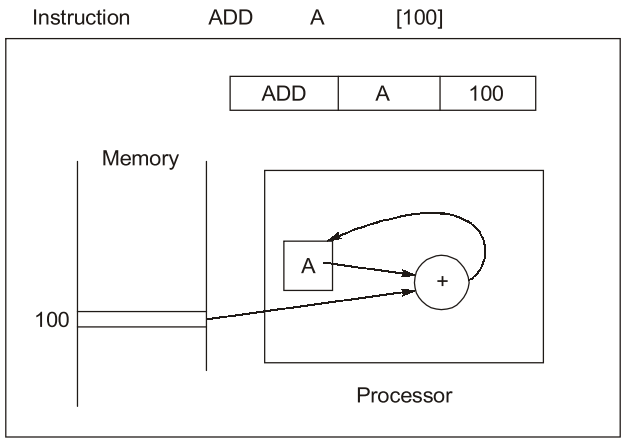
2.3.2 Two address Instruction

2-Address Instruction has one opcode and two address fields.



Two Address Instruction Format

Example: Instruction ADD A, [100]



Disadvantage of two address instructions: It may need three memory accesses (using all operands as memory addresses for arithmetic operations, ADD [200] [100]).

Student's Assignment

Q.1 Consider the following register-transfer language

$$R_3 \longleftarrow R_3 + M[R_1 + R_2]$$

where R_1, R_2 are the CPU registers and M is a memory location in primary memory. Which addressing mode is suitable for above register-transfer language?

(a) immediate (b) indexed
(c) direct (d) displacement

Q.2 In a 16-bit instruction code format 3-bit operation code, 12-bit address and 1 bit is assigned for address mode designation. For indirect addressing, the mode bit is

(a) 0 (b) 1
(c) pointer (d) off-set

Q.3 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. $Regs[R_4] \leftarrow Regs[R_4] + Regs[R_3]$
B. $Regs[R_4] \leftarrow Regs[R_4] + 3$
C. $Regs[R_4] \leftarrow Regs[R_4] + Mem[Regs[R_1]]$

List-II

1. immediate
2. register
3. displacement

Codes:

	A	B	C
(a)	3	2	1
(b)	2	1	3
(c)	1	2	3
(d)	None of these		

Q.4 Addressing mode is _____.

(a) explicitly specified
(b) implied by the instruction
(c) both (a) and (b)
(d) Neither (a) nor (b)

Q.5 Relative Addressing Mode is used to write Position-Independent code because

(a) the code in this mode is easy to atomize.
(b) the code in this mode is easy to make resident.
(c) the code in this mode is easy to relocate in the memory.
(d) code executes faster in this mode.

Q.6 The register which holds the address of the location to or from which data are to be transferred is known as

(a) index register
(b) instruction register
(c) memory address register
(d) memory data register

Q.7 Which of the following data transfer mode takes relatively more time?

(a) DMA (b) interrupt initiated I/O
(c) programmed I/O (d) isolated I/O

Q.8 Halt operation comes under _____ .

(a) data transfer (b) control transfer
(c) conversion (d) I/O transfer

Q.9 In four-address instruction format, the number of bytes required to encode an instruction is (assume each address requires 24 bits, and 1 byte is required for operation code)

(a) 9 (b) 13
(c) 14 (d) 12

Q.10 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	List-II
A. MOV X, R1	1. Three-address instruction
B. STORE X	2. Zero-address instruction
C. POP X	3. One-address instruction
	4. Two-address instruction

Codes:

	A	B	C
(a)	4	3	2
(b)	3	2	1
(c)	2	3	4
(d)	None of these		

Q.11 The register which keeps track of the execution of a program and which contains the memory