POSTAL BOOK PACKAGE 2025

CONTENTS

ELECTRICAL ENGINEERING

Objective Practice Sets

Analog Electronics

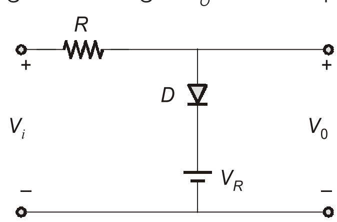
1 CHAPTER Basics of Semiconductor Diodes

MCQ and NAT Questions

Q.1 A diode whose terminal characteristics are related as $i_D = I_s e^{V/V_T}$, where I_s is the reverse saturation current and V_T is thermal voltage (V_T = 25 mV), is biased at I_D = 4 mA. Its dynamic resistance is

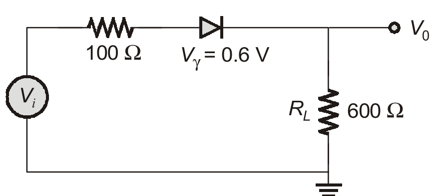
(a) 12.5 Ω (b) 50 Ω
(c) 6.25 Ω (d) 25 Ω

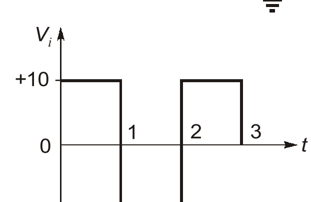
Q.2 In the circuit shown below the input V_i has positive and negative swings. V_o is the output.



(a) V_o = 0 for negative V_i
(b) $V_o = V_R$ for positive V_i
(c) $V_o = V_R$ for $V_i > V_R$
(d) $V_o = V_R$ for all V_i

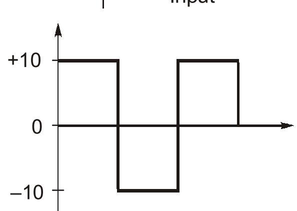
Q.3 In the circuit shown below, if the input voltage V_i is as shown below then the corresponding output waveform will be



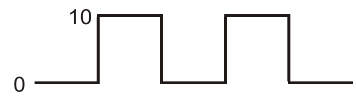


Input

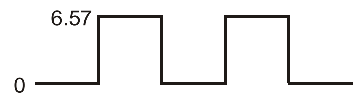
(a)



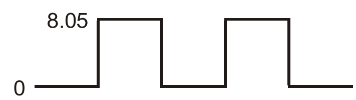
(b)



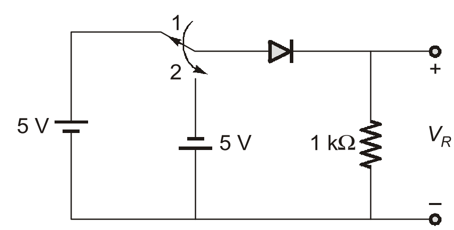
(c)



(d)

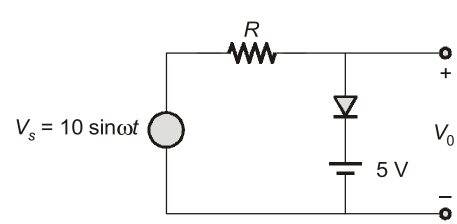


Q.4 In the circuit shown below, the switch was connected to position 1 at $t < 0$ and at $t = 0$, it is changed to position 2. Assume that the diode has zero voltage drop and a storage time t_s. For $0 < t \le t_s$, V_R is given by (all in Volts)

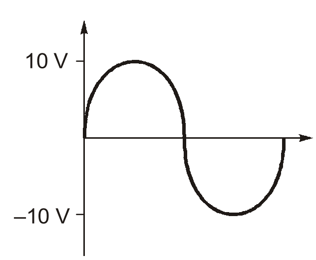


(a) $V_R = -5$ (b) $V_R = 0$
(c) $0 \le V_R < 5$ (d) $-5 < V_R < 0$

Q.5 For the circuit shown below assuming ideal diode, the output waveform V_0 is



(a)



Answers — Basics of Semiconductor Diodes

1. (c)	2. (c)	3. (d)	4. (a)	5. (d)	6. (c)	7. (b)	8. (b)
9. (a)	10. (c)	11. (d)	12. (4)	13. (0)	14. (d)	15. (a)	16. (a)
17. (c)	18. (c)	19. (a)	20. (c)	21. (d)	22. (c)	23. (b)	24. (b)
25. (a)	26. (d)	27. (c)	28. (a)	29. (c)	30. (c)	31. (d)	32. (d)
33. (b)	34. (b)	35. (d)	36. (c)	37. (a)	38. (b)	39. (a)	40. (c)
41. (d)	42. (b)	43. (d)	44. (b)	45. (d)	46. (b)	47. (a)	48. (d)
49. (b)	50. (d)	51. (b)	52. (c)	53. (d)	54. (b)	55. (a)	56. (a)
57. (b)	58. (d)	59. (b)	60. (b)	61. (c)	62. (c)	63. (c)	64. (500)
65. (1.048)	66. (b)	67. (d)	68. (b)	69. (b)	70. (c)	71. (d)	72. (b)
73. (a)	74. (c)	75. (b)	76. (b)	77. (d)	78. (d)	79. (a)	80. (d)
81. (b)	82. (b)	83. (c)	84. (d)	85. (c)	86. (c)	87. (b)	88. (a)
89. (b)	90. (d)	91. (c)	92. (d)	93. (b)	94. (c)	95. (b)	96. (c)
97. (a)	98. (b)	99. (c)	100. (a)	101. (b)	102. (a)	103. (a)	104. (c)
105. (0.12)	106. (40)	107. (10)	108. (b)	109. (c,d)	110. (a,b,c,d)	111. (a,b,c,d)	112. (a,d)

Explanations — Basics of Semiconductor Diodes

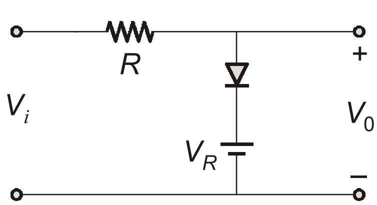
1. (c)

$$\frac{1}{r_d} = \frac{\partial I_D}{\partial V} = \frac{I_D}{V_T}$$

r_d : dynamic resistance.

$$\therefore \quad r_d = \frac{V_T}{I_D} = \frac{25}{4} = 6.25\ \Omega$$

2. (c)



Considering ideal diode :

for $V_i < V_R$, diode is OFF hence there is no current through R and $V_0 = V_i$.

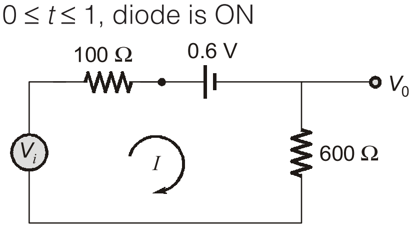
For $V_i > V_R$, diode is ON hence

$$V_0 = V_R$$

(as diode will act as short circuit)

3. (d)

For $0 \le t \le 1$, diode is ON



$$I = \frac{V_i - 0.6}{100 + 600} = \frac{10 - 0.6}{700}$$

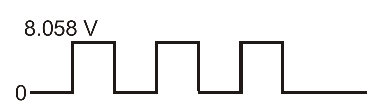
$$= 0.01343 \text{ A}$$

$$\therefore \quad V_0 = 600 \times 0.01343 = 8.058 \text{ V}$$

For $1 < t < 2$, diode is OFF, there will be no current in the circuit and hence

$$V_0 = 0 \text{ V}$$

Hence output waveform can be given as shown below:



4. (a)

For $0 < t < t_s$ diode will remain ON and hence

$$V_R + 5 = 0$$

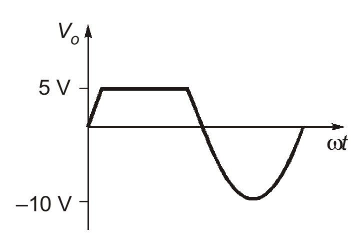
$$\therefore \quad V_R = -5 \text{ V}$$

5. (d)

For $0 \le V_i < V_R$ = diode is OFF $\Rightarrow V_0 = V_i$

For $V_R \le V_i \Rightarrow$ diode is ON $\Rightarrow V_0 = 5$ V

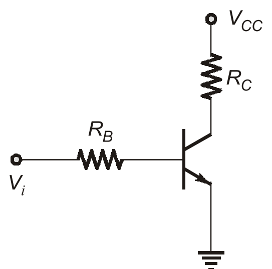
Hence output waveform can be as shown below



2 CHAPTER Bipolar Junction Transistors and Characteristics

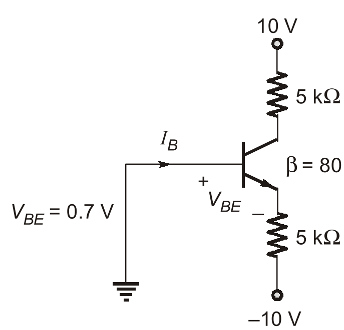
MCQ and NAT Questions

Q.1 In the transistor circuit shown, give the reason for collector to ground voltage to be V_{CC}.



(a) Collector emitter terminals shorted
(b) Collector resistance open circuit
(c) Input voltage V_i is negative
(d) Collector base terminal shorted.

Q.2 Find the value of base current in the circuit ____ μA.

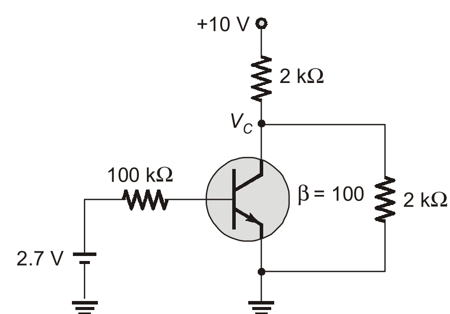


Q.3 **Assertion (A):** A self-biased BJT circuit is more stable as compared to a fixed biased one.
Reason (R): A self-biased BJT circuit uses more components as compared to a fixed biased one.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

Q.4 **Assertion (A):** In a transistor switching circuit, it is desirable that the transistor should not be driven into hard saturation for fast switching applications.
Reason (R): When a transistor is under saturation on state, both its emitter-base and collector-base junctions remain under forward bias.
(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

Q.5 A transistor has I_B = 100 μA and I_C = 2 mA. If I_B changes by 25 μA and I_C changes by 0.6 mA, the change in the value of β would be
(a) 3/2 (b) 5/4
(c) 1/4 (d) 4/5

Q.6 The value of V_C for the transistor shown in figure below is



(a) 3 volt (b) $\frac{1}{2}$ volt
(c) 2 volt (d) none of these

Q.7 A BJT biased in active region with *B-E* junction forward biased V_{BE} = 0.7 V. The 'β' of transistor to be 49. Assuming limiting case of $V_{CE} \le \frac{V_{CC}}{2}$, find $\frac{R_B}{R}$ = ______.