POSTAL BOOK PACKAGE 2024

ELECTRICAL ENGINEERING

CONVENTIONAL Practice Sets

CONTENTS

COMPUTER FUNDAMENTALS

1 CHAPTER

Digital Logic

Q.1 Find the minimum product of sums of the following expression:

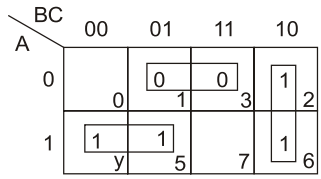
$$f = ABC + \bar{A}\bar{B}\bar{C}$$

Solution:

In order to find the minimum product of sums we must calculate what are the max terms.

We have SOP function as:

$$f = ABC + \bar{A}\bar{B}\bar{C}$$



$\Rightarrow$ Minimum terms are (0, 7)

Thus, maximum terms = (1, 2, 3, 4, 5, 6)

By using K-map

Hence, minimum product of sum will be $(\bar{A}+B)(A+\bar{C})(\bar{B}+C)$

Q.2 Show with the help of a block diagram represent Boolean function:

$$f = AB + BC + CA$$

can be realised using only 4 : 1 multiplexer.

Solution:

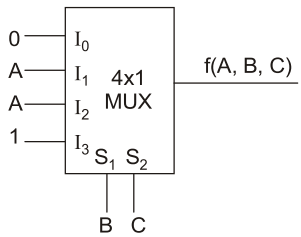
$f = AB + BC + CA$

A \ BC	00	01	11	10
0	0 0	0 1	1 3	0 2
1	0 4	1 5	1 7	1 6

Using MSB method:

	I_0	I_1	I_2	I_3
$\bar{A}$	0	1	2	③
A	4	⑤	⑥	⑦
	0	A	A	1

Implementing $f(A, B, C)$ using 4×1 MUX



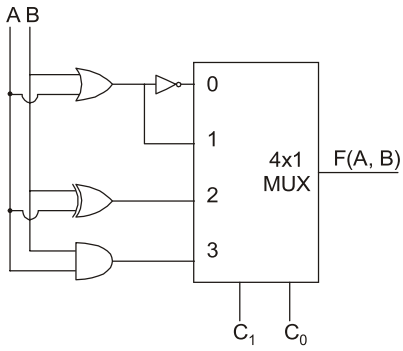
Q.3 A logic network has two data inputs A and B, and two control inputs C_0 and C_1. It implements the function F according to the following table.

C_1	C_0	F
0	0	$\overline{A+B}$
0	1	$A+B$
1	0	$A \oplus B$
1	1	AB

Implement the circuit using one 4 to 1 Multiplexer, one 2-input Exclusive OR gate, one 2-input AND gate, one 2-input OR gate and one Inverter.

Solution:

I_0 will gets activated when both the select lines are zero thus I_0 will intake $\overline{A+B}$.
I_1 will gets activated when C_1 is 0 and C_0 is 1 thus I_1 will intake $A + B$.
Similarly, I_2 will intake $A \oplus B$ and I_3 will intake AB.



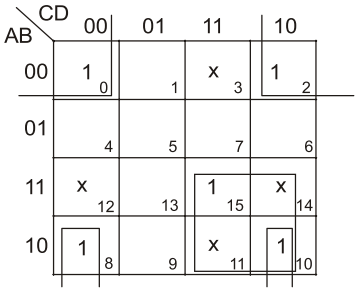
Q.4 Find the minimum sum of products form of the logic function.

$$f(A, B, C, D) = \Sigma m(0, 2, 8, 10, 15) + \Sigma d(3, 11, 12, 14)$$

Where m and d denote the min-terms and don't cares respectively.

Solution:

$$f(A, B, C, D) = \Sigma m(0, 2, 8, 10, 15) + \Sigma d(3, 11, 12, 14)$$



The minimum SOP form of the logic function is given as: $f(A, B, C, D) = B'D' + AC$.

Q.5 Express the function $f(x, y, z) = xy' + yz'$ with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.

Solution:

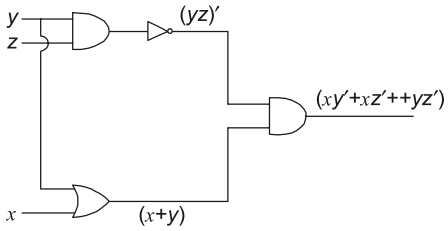
To use only single NOT gate, express it with only one complementation and one or more AND/OR operations.

$$f(x, y, z) = xy' + yz'$$

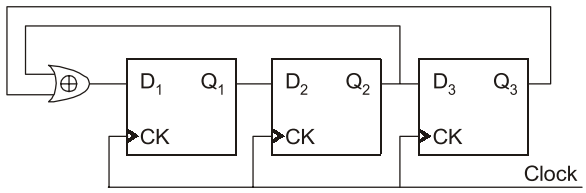
Add reduced term to f

$$f(x, y, z) = xy' + yz' + xz'$$
$$= yz' + x(y' + z')$$
$$= y(y' + z') + x(y' + z')$$
$$= (x + y)(y' + z') = (x + y)(yz)'$$

Thus the given function has been represented using one complement operation with complement on *yz*.
Logic circuit implementing the expression obtained is given as below:



Q.6 Consider the synchronous sequential circuit in figure.



(a) Draw a state diagram which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

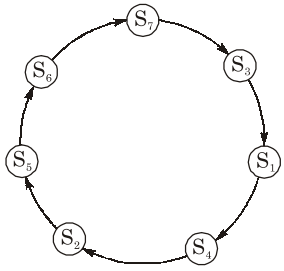
0	0	0	S_0
0	0	1	S_1
0	1	0	S_2
0	1	1	S_3
1	0	0	S_4
1	0	1	S_5
1	1	0	S_6
1	1	1	S_7

(b) Given that the initial state of the circuit is S_4, identify the set of states which are not reachable.

Solution:

$D_1(Q_2 \oplus Q_3)$	$D_2(Q_1)$	$D_3(Q_2)$	Q_1	Q_2	Q_3	*State*
			1	1	1	(S_7)
0	1	1	0	1	1	(S_3)
0	0	1	0	0	1	(S_1)
1	0	0	1	0	0	(S_4)
0	1	0	0	1	0	(S_2)
1	0	1	1	0	1	(S_5)
1	1	0	1	1	0	(S_6)
1	1	1	1	1	1	(S_7)

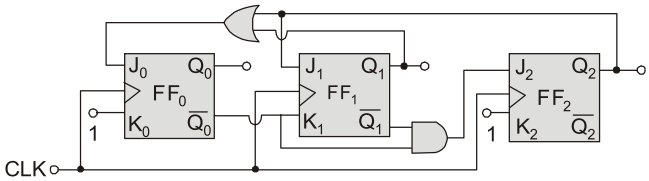
(a) The state diagram which is implemented by the circuit is as follows:



(b) If the initial state of the circuit is S_4, then the state which is not reachable is S_0

$S_4 \rightarrow S_2 \rightarrow S_5 \rightarrow S_6 \rightarrow S_7 \rightarrow S_3 \rightarrow S_1$

Q.7 For the synchronous counter shown in figure write the truth table of Q_0, Q_1 and Q_2 after each pulse starting from $Q_0 = Q_1 = Q_2 = 0$ and determine the counting sequence and also the modulus of the counter.



What is the modulus of the counter with initial state $Q_2\ Q_1\ Q_0 = 000$?

(a) 3 (b) 4

(c) 5 (d) 6

Solution: (c)

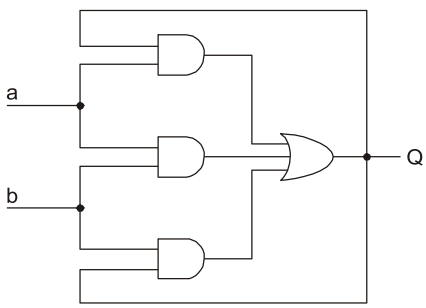
J_2 $(\bar{Q}_0\ \bar{Q}_1)$	K_2 (1)	J_1 (Q_2)	K_1 $(\bar{Q}_0)$	J_0 $(Q_1 + Q_2)$	K_0 (1)	Q_2	Q_1	Q_0
Initially						0	0	0
1	1	0	1	0	1	1	0	0
1	1	1	1	1	1	0	1	1
0	1	0	0	1	1	0	1	0
0	1	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0	0

There are 5 different states in the synchronous counter.

Therefore, the modulus of the counter is 5.

Q.8 Analyse the circuit in figure and complete the following table:

a	b	Q_n
0	0	
0	1	
1	0	
1	1	



Solution:

The output of the circuit is given as

$$Q_n = aQ_{n-1} + ab + bQ_{n-1}$$
$$Q_n = Q_{n-1}(a + b) + ab$$

a	b	Q_n
0	0	0
0	1	Q_{n-1}
1	0	Q_{n-1}
1	1	1

Q.9 Difference between Mealy and Moore state Machine.

Solution:

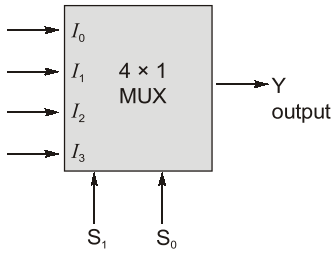
(a) Mealy and Moore Models are the basic Models of state Machines. A state machine which uses only entry actions, so that its output depends on the state, is called a Moore model. A state machine which uses only input actions, so that the output depends on the state and also on inputs, is called a Mealy models. The Models selected will influence a design but there are no general indications as to which model is better choice of a Model depends on the applications, executions means (for instance, hardware systems are usually best realized as Moore Models) and personal preferences of a designer or programmer.

(b) Mealy machine has outputs that depend on the state and input (thus, the FSM has the output written on edges) Moore machine has outputs that depend on state only. Thus, the FSM has the output written in the state itself.

Q.10 Explain in brief about multiplexers, with circuit diagram.

Solution:

It is combinational circuit which have many data inputs and single output depending on control or select lines. For N input lines, log n (base 2) selections lines, or we can say that for 2^n input lines, n selection lines are required. Multiplexers are also known as "Data n selector or parallel to serial convertor or Many to one circuit or universal logic circuit". Multiplexers are mainly used to increase amount of the data that can be sent over the network within certain amount of time and bandwidth.



Now, the implementations of 4 : 1 Multiplexer using truth table and gates is shown below:

Truth table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

So final equation, $Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$