# Electrical Engineering

# Power Electronics

Comprehensive Theory

*with* Solved Examples and Practice Questions

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# Contents

## Power Electronics

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CHAPTER 2

# Power Semi-conductor Diode and Transistor

## 2.1 Basic Semiconductor Physics Important Concepts are as follows:

- Current in a semiconductor is carried by both electrons and holes.
- Electron and holes move by both drift and diffusion.
- Intentional doping of the semiconductor with impurities will cause the density of holes and electrons to be vastly different.
- The density of minority carriers increases exponentially with temperature.
- A *pn* junction can be formed by doping one region *n*-type and the adjacent region *p*-type.
- A potential barrier is set up across a pn junction in thermal equilibrium that balances out the drift and diffusion of carriers across the junction so that no net current flows.
- In reverse bias a depletion region forms on both sides of the *pn* junction and only a small current can flow by drift.
- In forward bias large numbers of electrons and holes are injected across the *pn* junction and large currents flow by diffusion with small applied voltages.
- Large numbers of excess electron-hole pairs are created by impact ionization if the electric field in the semiconductor exceeds a critical value.
- Avalanche breakdown occurs when the reverse-bias voltage is large enough to generate the critical electric field $E_{BD}$.

## 2.2 Basic Structure and I-V Characteristics

The practical realization of diode for power application is shown below.

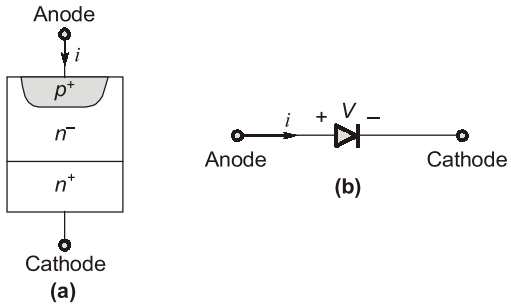



***Figure*-2.1**

It consists of a heavily doped *n*-type substrate on top which is grown a lightly doped '$n^-$' epitaxial layer of specified thickness. Finally, the *p*-*n* junction is formed by diffusing in a heavily doped p-type region that forms the anode of the diode.

The $n^-$ layer which is often termed the drift region, is the prime structural feature not formed in low power diodes. Its function is to absorb the depletion layer of the reverse biased $p^+$ $n^-$ junction.

This relatively long lightly doped region would appear to add significant ohmic resistance to the diode when it is forward biased.

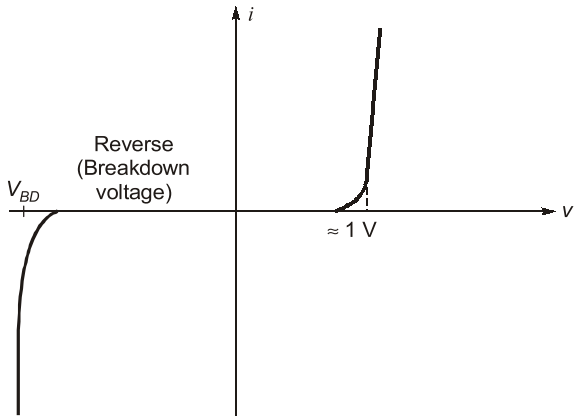



***Figure*-2.2**

The current grows linearly with the forward bias voltage rather than exponentially.

In reverse bias only a small leakage current, which is independent of the reverse voltage, flows until the reverse break down voltage $V_{BD}$ is reached. When breakdown is reached the voltage appears to remain essentially constant while the current increases dramatically.

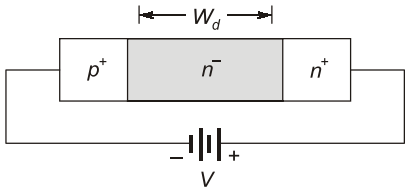



***Figure*-2.3**

If the length $W_d$ of the lightly doped region is longer than the depletion layer width at breakdown, then the structure is termed a non punch through diode, that is, the depletion layer has not reached through (or punched through) the lightly doped drift region and reached the highly doped $n^+$ subtract.

Two basic facts; first, large breakdown voltages require lightly doped junctions, at least on one side. Second, the drift layer in the diode must be fairly long in high voltage devices to accommodate the long depletion layers.

## Switching Characteristics

A power diode requires a finite time to switch from the blocking state (reverse bias) to the on state (forward bias) and vice versa.

The features of particular interest in these waveforms are the voltage overshoot during turn on and the sharpness of the fall of the reverse current during the turn off phase.

The overshoot of the voltage during turn on is not observed with signal level diodes.

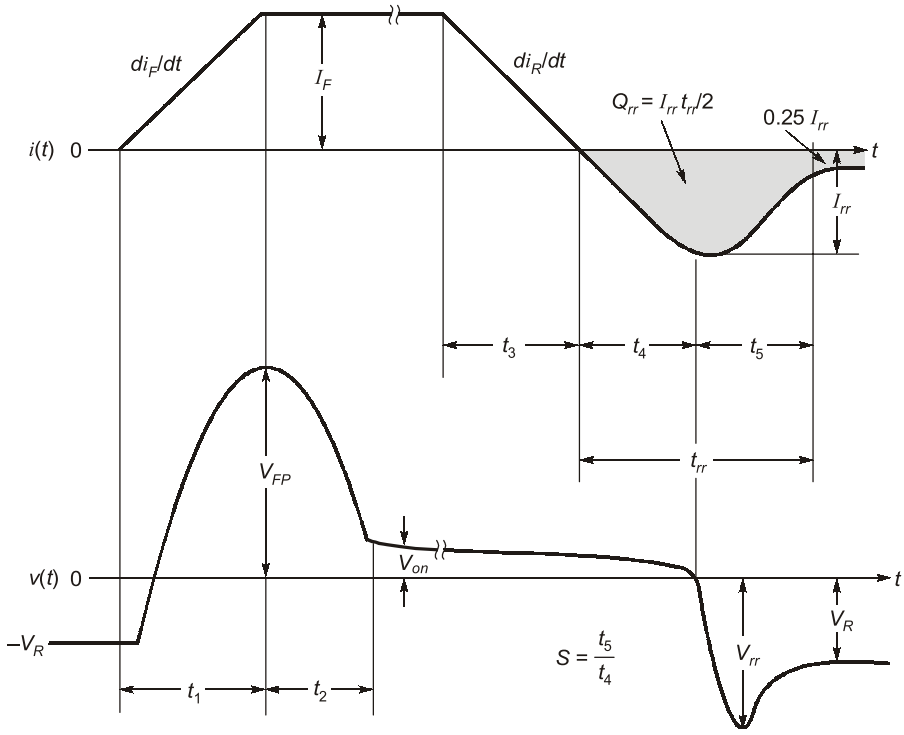



***Figure*-2.4**

## Turn-on Transient

The turn on portion of the diode waveform is encompassed by the times labeled $t_1$ and $t_2$. During these intervals two physical process occur in sequence. First the space charge stored in the depletion region (located mainly in the drift region) because of the large reverse bias voltage is removed (discharged) by the growth of the forward current. When the depletion layer is discharged to its thermal equilibrium level, the metallurgical junction becomes forward biased and the injection of excess carriers across the junction into the drift region commences at time $t_1$, thus marking the start of the second phase and the end of the first. During the second phase, the excess-carrier distribution in the drift region grows towards the steadily state value that can be supported by the forward diode current $I_f$.

**NOTE:** Excess carries are injected into the drift region from both ends with holes being injected from the $p^+ n^-$ junction and electrons from the $n^+ n^-$ junction.

## Turn-off Transient

The turn off portion of the switching waveform is encompassed by the times labeled $t_3$, $t_4$ and $t_5$ and is essentially the inverse of the turn on process. First the excess carriers stored in the drift region must be removed before the metallurgical junctions can become reverse biased.

Once the carriers are removed by the combined action of recombination and sweep out by negative diode currents, the depletion layer acquires a substantial amount of space charge from the reverse bias voltage and expands into the drift region from both ends (junctions).

As long as there are excess carriers at the ends of the drift region, the $p^+ n^-$ and $n^+ n^-$ junctions must be forward biased. Thus, the diode voltage will little change from its on state value except for a small decrease due

to ohmic drops caused by the reverse current. But after the current goes negative and carrier sweep-out has proceeded for a sufficient time ($t_4$) to reduce the excess carriers density at both junctions to zero, the junctions become reverse biased. At this point the diode voltage goes negative and rapidly acquires substantial negative values as the depletion regions from the two junctions expand into the drift region towards each other.

The diode current ceases its growth in the negative direction and quickly falls, becoming zero after a time $t_5$.

The reverse current has its maximum reverse value, $I_{rr}$, at the end of the $t_4$ interval.

## Reverse Recovery

The time interval $t_{rr} = t_4 + t_5$ shown in the graph is often termed the reverse recovery time. Its characteristics are important in almost all power electronic circuits where diode are used.

$t_{rr}$ = reverse recovery time

$Q_{rr}$ = reverse recovery charge

$\frac{di_R}{dt}$ = rate of change of reverse current

$S$ = snappiness factor or softness factor

There quantities are inter related to each other.

We note that $I_{rr}$ can be written as

$$I_{rr} = \frac{di_R}{dt} \times t_4$$

$\because$ $$\boxed{s = \frac{t_5}{t_4}}$$

$$t_4 = t_{rr} - t_5 = \frac{t_{rr}}{s+1}$$

$\therefore$ $$I_{rr} = \frac{di_R}{dt} \times \frac{t_{rr}}{s+1}$$

$$\boxed{Q_{rr} \cong \frac{1}{2} I_{rr} t_{rr}}$$

So that, $$Q_{rr} = \frac{di_R}{dt} \frac{t_{rr}^2}{2(s+1)}$$

Reverse recovery time, $$\boxed{t_{rr} = \sqrt{\frac{2Q_{rr}(1+s)}{\left(\frac{di_R}{dt}\right)}}} \; ; \quad \boxed{I_{rr} = \sqrt{\frac{2Q_{rr}\left(\frac{di_R}{dt}\right)}{(s+1)}}}$$

The charge $Q_{rr}$ represents the portion of the total charge $Q_F$ (the charge stored in the diode during forward bias), which is swept out by the reverse current and not lost to internal recombination. Most of $Q_F$ is stored in the drift region.

**Example - 2.1** A power diode is in the forward conduction mode and the forward current is now decreased. The reverse recovery time of the diode is tr and the rate of fall of the diode current is *di/dt*. What is the stored charge?

(a) $\left(\frac{di}{dt}\right)\cdot t_r$

(b) $\frac{1}{2}\left(\frac{di}{dt}\right)\cdot t_r^2$

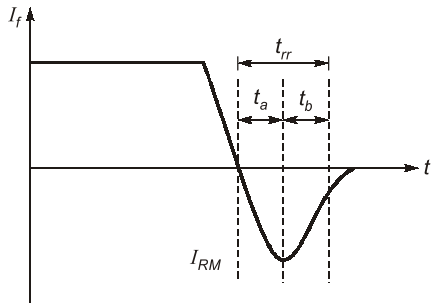
(c) $\left(\frac{di}{dt}\right)\cdot t_r^2$

(d) $\frac{1}{2}\left(\frac{di}{dt}\right)\cdot t_r$

***Solution : (b)***

From figure,

$$I_{RM} = t_a \frac{di}{dt}$$



Reverse Recovery Characteristic

Assuming reverse recovery characteristics to be triangular, storage charge $Q_R$

$$Q_R = \frac{1}{2} I_{RM}\, t_{srr} = \frac{1}{2}\left(t_a \frac{di}{dt}\right) t_{rr}$$

if $t_a \approx t_{rr}$

$$Q_R = \frac{1}{2}\left(\frac{di}{dt}\right) t_{rr}^2$$

## Schottky Diodes: Structure and I-V Characteristics

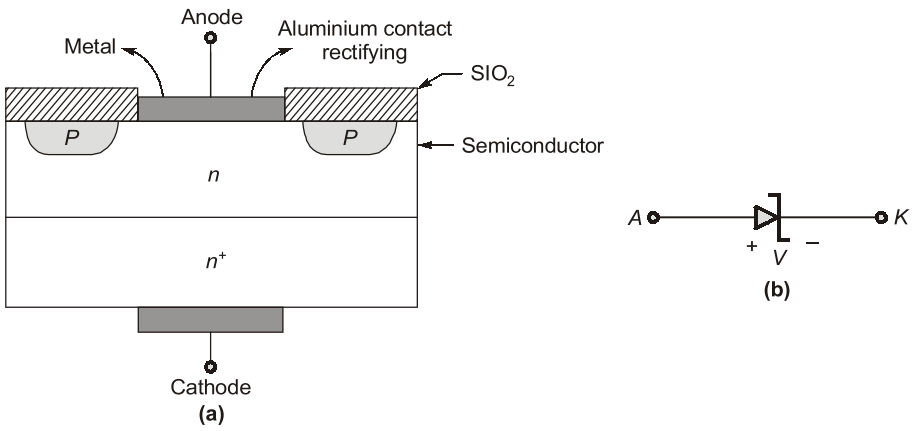



***Figure*-2.5**

A metal semiconductor junction is established. When the materials are joined, the electrons in the *n*-type silicon semiconductor material immediately flow into the adjoining metal, establishing a heavy flow of majority carriers. Since the injected carriers have a very high kinetic energy level compared to the electrons of the metal, they are commonly called **"hot carriers"**.

In the conventional p-n junction, there was the injection of minority carriers into the adjoining region. Here the electrons are injected into a region of the same electron polarity. Schottky diodes are therefore unique in that, conduction is entirely by majority carriers.

The heavy flow of electrons into the metal creates a region near the junction surface depleted of carriers in the silicon material much like the depletion region in the *p-n* junction diode. The additional carriers in the metal establish a **'negative wall'** in the metal at the boundary between the two materials. The net result is a 'surface barrier' between the two materials, preventing any further current.

The application of forward bias will reduce the strength of the negative barrier. The result is a return to the heavy flow of electrons across the boundary, the magnitude of which is controlled by the level of the applied bias potential.

The barrier at the junction for a schottky diode is less than that of the *p-n* junction device in both the forward and reverse bias regions. The result is therefore a higher current at the same applied bias in the forward and reverse bias regions. This is a desirable effect in the forward bias region but highly undesirable in the reverse bias region.

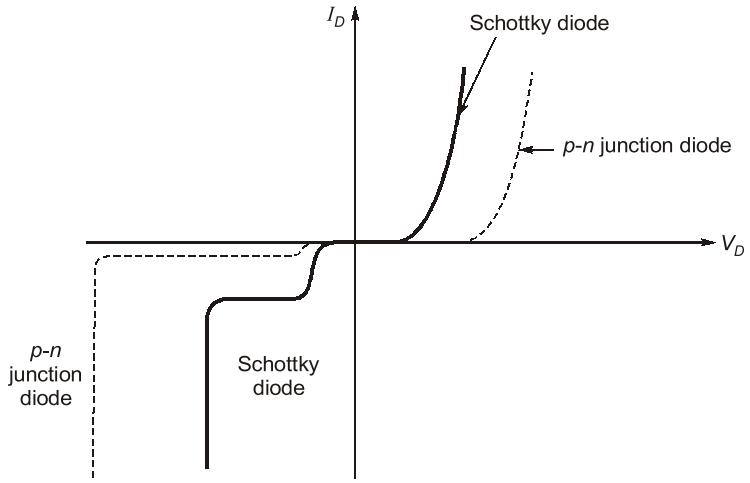



***Figure*-2.6 :** *Comparison of characteristics of schottky diode and p-n junction diode*

The absence of minority carriers at any appreciable level in the schottky diode results in a reverse recovery time of significantly lower levels, this is the primary reason schottky diodes are so effective at frequencies approaching 20 GHz, where the device must switch states at a very high rate.

**Points to Remember in Power Semiconductor Diodes**

- Power diodes are constructed with a vertically oriented structure that includes a *'$n^-$'* drift region to support large blocking voltages.
- The breakdown voltage is approximately inversely proportional to the doping density of the drift region, and the required minimum length of the drift region scales with the desired breakdown voltage.
- Achievement of large breakdown voltages requires special depletion layer boundary shaping techniques.
- Conductivity modulation of the drift region in the on state keeps the losses in the diode to manageable levels even for large on-state currents.
- Low on-state losses require long carrier lifetimes in the diode drift region.
- Minority-carrier devices have lower on-state losses than majority-carrier devices such as MOSFETs at high blocking voltage ratings.
- During the turn-on transient the forward voltage in a diode may have a substantial overshoot, on the order of tens of volts.
- Short turn-off times require short carrier lifetimes, so a trade-off between switching times and on-state losses must be made by the device designer.
- During turn-off, fast reverse recovery may lead to large voltage spikes because of stray inductance.

- The problems with the reverse-recovery transient are most severe in diodes with large blocking voltage ratings.
- Schottky diodes turn on and off faster than *pn*-junction diodes and have no substantial reverse-recovery transient.
- Schottky diodes have lower on-state losses than *pn*-junction diodes but also have low breakdown voltage ratings, rarely exceeding 100 V.

## 2.3 Power Bipolar Junction Transistor : (Power BJT)

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power Bipolar Junction Transistor (BJT) must have a substantially different structure than its logic level counterpart. The modified structure leads to significant differences in I-V characteristics.

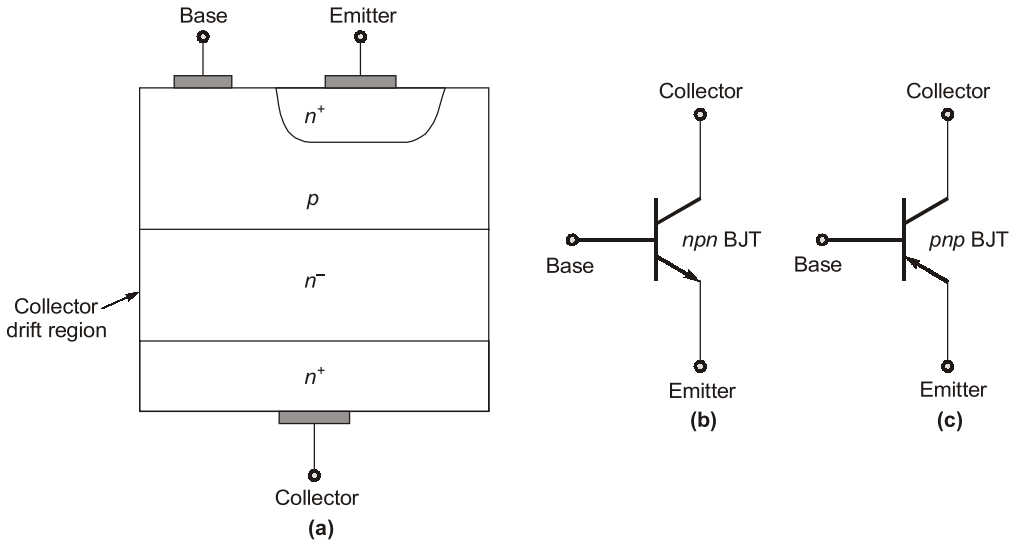



***Figure*-2.7**

In most power applications, the base is the input terminal, the collector is the output terminal, and the emitter is common between input and output (the so called common emitter configuration). A *pnp* transistor, whose circuit symbol is shown above, would have the opposite type of doping in each of the layers shown in the figure.

**NOTE:** *npn* transistors are much more widely used than *pnp* transistor as power switches.

The vertical structure is preferred for power transistors because it maximizes the cross sectional area through which the current in the devices is flowing. This minimizes the on state resistance and thus the power dissipation in the transistor. In addition, having a large cross sectional area minimizes the thermal resistance of the transistor, thus also helps to keep power dissipation problems under control. The doping levels in each of the layers and the thickness of the layers have a significant effect on the characteristics of the device. The doping in the emitter layer is quite large, where as the base doping is moderate. The $n^-$ region that forms the collector half of the *C-B* (collector base) junction is usually termed the collector drift region and has a light doping level. The $n^+$ region that terminates the drift region has a doping level similar to that found in the emitter.

**NOTE:** The thickness of the drift region determines the breakdown voltage of the transistor.

## I-V Characteristics

The output characteristics ($I_C$ versus $V_{CE}$) of a typical *npn* power transistor are shown above. The various curves are distinguished from each other by the value of the base current. There is a maximum collector-emitter voltage that can be sustained across the transistor when it is carrying substantial collector current. This voltage is usually labeled $BV_{SUS}$. In the limit of zero base current, the maximum voltage between collector and emitter that can be sustained increase some what to a value labeled $BV_{CEO}$, the collector emitter breakdown voltage when the base is open circuited. This voltage is measure of the transistor's voltage standoff capability because usually the only time the transistor will see large voltages is when the base current is zero and the BJT is in cut-off.

The voltage $BV_{CBO}$ is the collector base breakdown voltage when the emitter is open circuited.

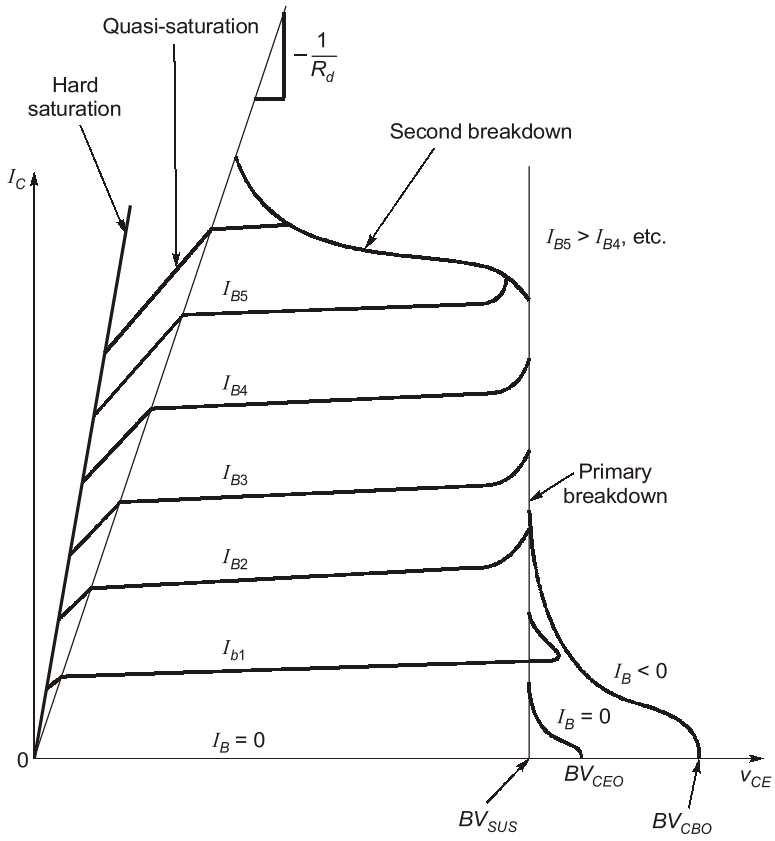


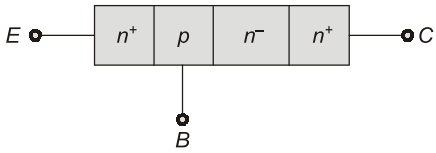

***Figure*-2.8**

The region labeled primary breakdown is due to conventional avalanche breakdown of the *C-B* junction and attendant large flow of current. This region of characteristics is to be avoided because of the large power dissipation that clearly accompanies such breakdown.

The major difference between the *i-v* characteristics of a power transistor and those of a logic level transistor is the region labeled Quasi-Saturation on the power transistor characteristics.

### Quasi-Saturation

To understand the phenomenon of quasi saturation, the collector drift region should be considered. It is assumed that the transistor is initially in the active region and now base current is allowed to increase.




There is a simultaneous increase in the voltage drop in the drift region as a result of its ohmic resistance because of the increase in $I_C$.

A very large number of electrons are supplied to the *C-B* junction via injection from the emitter and subsequent diffusion across the base. As this excess carriers build up in the drift region begins to occur, the quasi saturation region of the i-v characteristics is entered.

The ohmic resistance of the drift region is $R_d$, then the boundary between the quasi saturation region and the active region is given by

$$I_C = \frac{V_{CE}}{R_d}$$

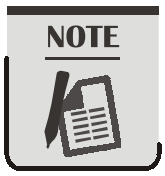
As the injected carriers increase, the drift region is gradually shorted out and the voltage across the drift region drops even though the collector current is large.

Hard saturation is obtained when the excess- carriers density reaches the other side of the drift region.

**Relation Between α and β**

Most of the electrons, proportional to $I_E$, given out by emitter, reach the collector. In other words, collectors current $I_C$, though less than emitter current $I_E$, is almost equal to $I_E$. A symbol α is used to indicate how close in value these two current are. Here α, called forward current gain, is defined as

$$\alpha = \frac{I_C}{I_E}$$




As $I_C < I_E$, value of a varies from 0.95 to 0.99. In transistor, base current is effectively the input current and collector current is output current. The ratio of collector (output) current $I_C$ to base (input) current $I_B$ is known as the current gain β.

$$\beta = \frac{I_C}{I_B}$$

Use of KCL, $I_E = I_C + I_B$

**NOTE:** The emitter current is the largest of three currents, collector current is almost equal to, but less than, emitter current. Base current has the least value.

Dividing both sides by $I_C$, we get

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

## BJT Switching Performance

When input voltage $V_B$ to base circuit is made $-V_2$ at $t_0$, junction $EB$ is reverse biased, $V_{BE} = -V_2$, the transistor is off, $i_B = i_C = 0$ and $V_{CE} = V_{CC}$.

At time $t_1$, base emitter voltage $V_{BE}$ begins to rise gradually from $-V_2$ and collector current $i_C$ begins to rise from zero and collector-emitter voltage $V_{CE}$ starts falling from initial value $V_{CC}$. After sometime delay $t_d$, called delay time, the collector current rises to 0.1 $I_{CS}$, $V_{CE}$ falls from $V_{CC}$ to 0.9 $V_{CC}$ and $V_{BE}$ reaches $V_{BES}$ = 0.7 V.

This delay time is required to charge the base emitter capacitance to $V_{BES}$ = 0.7 V.

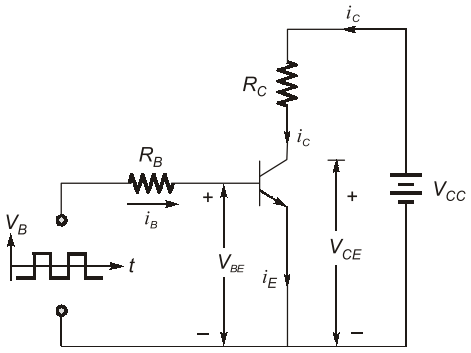



***Figure*-2.9**

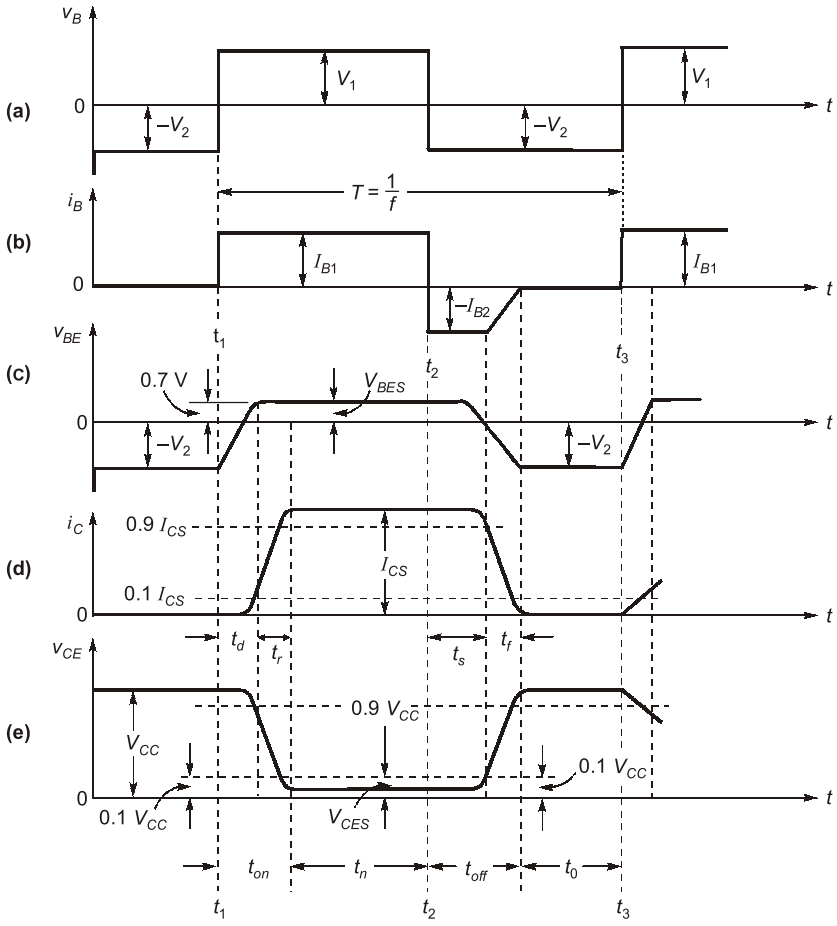
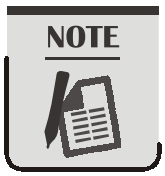
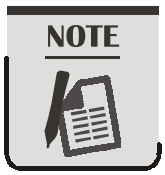



***Figure*-2.10**




- Thus, delay time ($t_d$) is defined as the time during which the collector current rises from zero to 0.1 $I_{CS}$ and collector emitter voltage falls from $V_{CC}$ to 0.9 $V_{CC}$. After delay time $t_d$, collector current rises from 0.1 $I_{CS}$ to 0.9 $I_{CS}$ and $V_{CE}$ falls from 0.9 $V_{CC}$ to 0.1 $V_{CC}$ in time $t_r$.
- This time $t_r$ is known as rise time which depends up on transistor junction capacitance. Rise time ($t_r$) is defined as the time during which collector current rises from 0.1 $I_{CS}$ to 0.9 $I_{CS}$ and collector emitter voltage falls from 0.9 $V_{CC}$ to 0.1 $V_{CC}$.
- The total turn on time is, $\boxed{t_{on} = t_d + t_r}$

In case to turn off a transistor, input voltage $V_B$ and input base current $i_B$ are reversed. At time $t_2$, input voltage $V_B$ to base circuit is revered from $V_1$ to $-V_2$. At the same time, base current changes from $I_{B1}$ to $-I_{B2}$ negative base current removes excess carriers from base.




- The time ($t_s$) required to remove these excess carriers is called storage time and only after $t_s$, base current $I_{B2}$ begins to decrease towards zero.
  Transistor comes out of saturation only after $t_s$.
- Storage time ($t_s$) is defined as the time during which collector current falls from $I_{CS}$ to 0.9 $I_{CS}$ and collector emitter voltage $V_{CE}$ rises from $V_{CES}$ to 0.1 $V_{CC}$. After $t_s$, collector current begins to fall and collector emitter voltage starts building up. Time ($t_f$) called fall time, is defined as the time during which collector current drops from 0.9 $I_{CS}$ to 0.1 $I_{CS}$ and collector emitter voltage rise from 0.1 $V_{CC}$ to 0.9 $V_{CC}$.

  Transistor turn off time, $\boxed{t_{off} = t_s + t_f}$

  $t_n$ = conduction period of transistor
  $t_o$ = off period
  $f$ = switching frequency

  $T = \frac{1}{f}$ is the period time

**Second Breakdown**

Bipolar junction transistor and to some degree other type of minority carrier devices have a potential failure mode, usually termed second breakdown. It appears on the output characteristics of the BJT as a sudden drop in the collector emitter voltage at large collector currents. As the collector voltage drops, there is often a significant increase in the collector current and a substantial increase in the power dissipation. This situation is particularly dangerous for the BJT because the dissipation is not uniformly spread over the entire volume of the device but is concentrated in highly localized regions where the local temperature may grow very quickly to unacceptably high values. It this situation is not terminated in a very short time, device destruction results.

This is clear from the fact that a drop in voltage accompanies second breakdown, where as no such drop is observed in avalanche breakdown. Several intrinsic aspects of the transistor combine to give the BJT its susceptibility to second breakdown. First there is the general tendency of minority carrier devices to thermal runaway when the voltage across them is held approximately constant as the device temperature increases. Minority carrier devices have a negative temperature coefficient of resistivity (the resistivity drops as the temperature increases because the minority carrier densities are proportional to the intrinsic carrier density $n_i$, which increases exponentially with temperature). This means the power dissipation will increase as the resistance drops as long as voltage remains constant. If the rate of increase in power dissipation with temperature is greater than linear

with temperature, then an unstable situation will result when the power dissipated exceeds the rate at which heat energy can be removed. This situation becomes a classic case of positive fed back in which the power dissipation leads to an increase in temperature, which leads to further increase in power dissipation, and so on, until device destruction results. It is often and quite approximately termed as thermal runaway.

The formation of the current filaments and subsequent localized thermal runaway requires only a non-uniformity in the current density and enough localized power dissipation to cause a substantial rise in the temperature of the filament. Indeed, the increase in carrier density in the current filament may often cause a drop in the external voltage in the device. When the shorting effect of the filament is strong enough to cause this voltage drop, the device is said to be in second breakdown.

**Safe Operating Area**

The safe operation area (SOA) of a power transistor specifies the safe operating limits of collector current $I_C$ versus collector emitter voltage $V_{CE}$. For reliable operation of the transistor, the collector current and voltage must always lie with in this area. Actually, two types of safe operating areas are specified by the manufacturers, *FBSOA* and *RBSOA*.

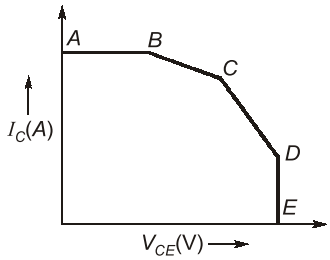


**Figure-2.11 (a)**

The forward biased safe operating area (FBSOA) pertains to the transistor operation when base emitter junction is forward biased to turn on the transistor. The scale for $I_C$ and $V_{CE}$ are logarithmic.

Boundary *AB* is the maximum limit for dc and continuous current for $V_{CE}$ less than about 80 V. For $V_{CE}$ for more than 80 V, collector current has to be reduced to boundary *BC* so as to limit the junction temperature to safe values for still higher $V_{CE}$, current should further be reduced so as to avoid secondary breakdown limit. Boundary *CD* defines this secondary breakdown limit. Boundary *DE* gives the maximum voltage capability for this particular transistor.

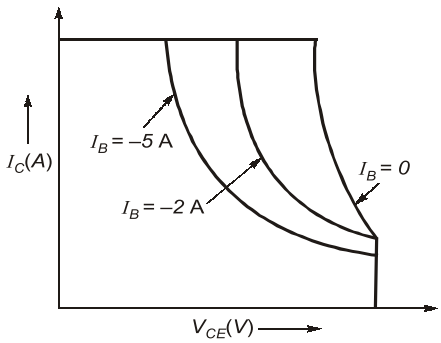


**Figure-2.11 (b)**

During turn-off, a transistor is subjected to high current and high voltage with base emitter junction reverse biased. Safe operating area for transistor during turn off is specified as reverse blocking safe operating area (*RBSOA*). *RBSOA* specifies the limits of transistor operation at turn-off when the base current is zero or when the base emitter junction is reverse biased (i.e. with base current negative). With increased reverse bias, area *RBSOA* decreases in size.

**Important conclusions in this topic are listed below:**

- The power BJT has a vertically oriented structure with a highly interdigitated B-E structure and a lightly doped collector drift region.
- The drift region determines the blocking voltage rating of the BJT and also cause the so-called quasi-saturation region of the I-V characteristics.
- The BJT is a normally-off device that is turned on by the application of sufficiently large base current to cause injection of large numbers of minority carriers into the base from the emitter region. The subsequent diffusion of these carriers across the base of the collector forms the collector current.
- Power BJTs have low current gain, especially at larger breakdown voltage ratings. This has led to the development of monolithic Darlington transistors, which have larger current gains.

- Lateral current flow in the base is the basic limiting factor in BJT performance. It cause lateral voltage drops, which lead to emitter current crowding, which in turn cause decreases in current gain. If the current crowding is excessive, second breakdown and device destruction will occur.
- Heavy conductivity modulation of the drift region in order to minimize on-state losses requires large carrier lifetimes. But this leads to long turn-off times, so a trade-off must be made in the design of the BJT between lower on-state losses or shorter switching times.
- Turn-off some types of BJTs should be done with a controlled rate of change of negative base current in order to avoid isolating excessive stored charge in the BJT, which would result in excessively long turn-off times and large power dissipation.
- The SOAs of the BJT are limited by second breakdown. The RBSOA is normally the limiting factor.
- BJTs with limited SOAs may require that their switching trajectory be controlled with snubber circuits during both turn-on and turn-off.

**Example - 2.2** Turn-on and turn-off times of transistor depend on

(a) static characteristic (b) junction capacitances

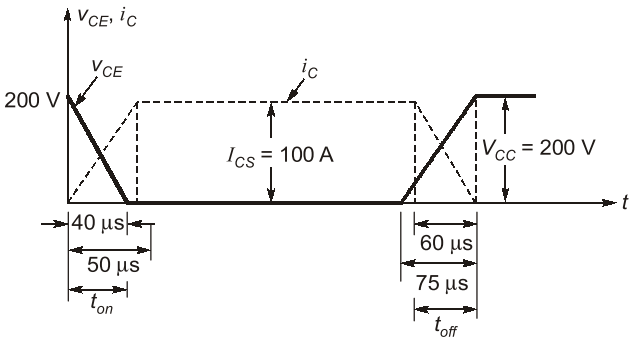
(c) current gain (d) none of the above

***Solution : (b)***

Turn-on and turn-off times of transistor depend on junction capacitance.

Because of charging and discharging of junction capacitance a transistor does not turn-on and turn off instantly.

**Example - 2.3** A power transistor has its switching waveforms as shown in figure. If the average power loss in the transistor is limited to 300 W, find the switching frequency at which this transistor can be operated.




***Solution :***

$$\text{Energy loss during turn-on} = \int_0^{t_{on}} i_C \cdot v_{CE}\, dt$$

$$= \int_0^{t_{on}} \left(\frac{I_{CS}}{50} \times 10^6 t\right)\left(V_{CC} - \frac{V_{CC}}{40} \times 10^6 t\right) dt$$

$$= \int_0^{t_{on}} (2 \times 10^6 t)\,(200 - 5 \times 10^6 t)\, dt \;= 0.1067 \text{ watt-sec}$$

$$\text{Energy loss during turn-off} = \int_0^{t_{off}} \left(100 - \frac{100}{60} \times 10^6 t\right)\left(\frac{200}{75} \times 10^6 t\right) dt = 0.1603 \text{ watt-sec}$$

Total energy loss in one cycle = 0.1067 + 0.1603 = 0.267 watt-sec

Average power loss in transistor = Switching frequency × Energy loss in one cycle

∴ Allowable switching frequency,

$$f = \frac{300}{0.267} = 1123.6 \text{ Hz}$$

## 2.4 Power MOSFET

A metal oxide semiconductor field effect transistor (MOSFET) has three terminals called drain (*D*), source (*S*) and gate (*G*).

The basic structure and circuit symbol of power MOSFET is,

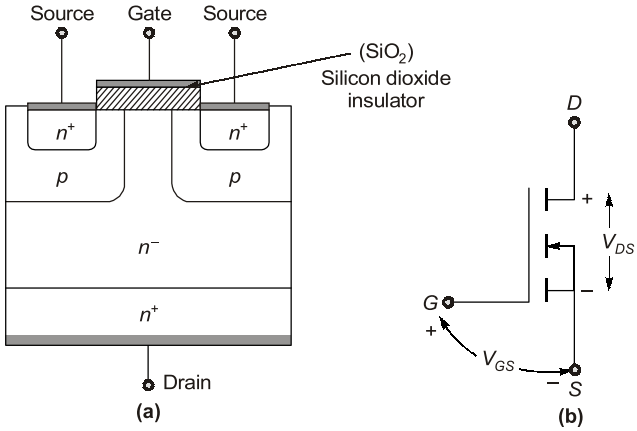



***Figure*-2.12**

- Generally MOSFETs are low voltage and high current devices.
- These are very popular in dc to dc conversion (choppers).
- These are very fast devices compared to BJT.
- BJT is a minority carrier device where MOSFET is a majority carrier device.
- MOSFET has a very high input impedance.
- Gate is insulated from the rest of the device.
- No steady current flows through the gate. (Only displacement current like in parallel plate capacitor will flow.)
- MOSFET is in cutoff region when gate to source voltage ($V_{GS}$) is less than threshold value.
- When $V_{GS}$ > Threshold ($V_{Th}$). It converts silicon surface below the gate into an N-type channel.
- The threshold value depends upon oxide layer and it can be reduced by reducing the thickness of $SiO_2$ layer.
- A BJT is a current controlled device where as a power MOSFET is a voltage controlled device.
- The control signal, or base current in BJT is much larger than the control signal (or gate current) required in a MOSFET. This is because of the fact that gate circuit impedance in MOSFET is externally high, of the order of $10^9$ ohm's. This large impedance permits the MOSFET gate to be driven directly from micro electronic circuits.

**NOTE:** BJT suffers from second breakdown voltage whereas MOSFET is free from this problem.