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CONTENTS

ELECTRONICS ENGINEERING

Objective Practice Sets

Computer Organization

1. Machine Instructions and Addressing Modes ..... 2 - 15

2. ALU, Data Path and Control Unit ..... 16 - 24

3. Instruction Pipelining ..... 25 - 38

1 CHAPTER
Machine Instructions and Addressing Modes

MCQ and NAT Questions

Q.1 The computer performs all mathematical and logical operations inside its

(a) Memory unit (b) Central processing unit
(c) Output unit (d) Visual display unit

Q.2 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Pointer
B. Position Independent code
C. Constant operand

List-II

1. Indirect AM
2. Immediate AM
3. Relative AM

Code:

	A	B	C
(a)	1	2	3
(b)	3	2	1
(c)	1	3	2
(d)	2	3	1

Q.3 The most appropriate matching of the following pairs is

Column 1	Column 2
X: Indirect addressing	1. Loops
Y: Immediate addressing	2. Pointers
Z: Auto-decrement address	3. Constant

(a) X-2, Y-3, Z-1 (b) X-3, Y-2, Z-1
(c) X-1, Y-3, Z-2 (d) X-3, Y-1, Z-2

Q.4 A processor can support a maximum memory of 4 GB where memory is word addressable and word is 2 bytes. What will be the size of the address bus of the processor?

(a) At least 2 bytes (b) At least 28 bits
(c) At least 31 bits (d) Minimum 4 bytes

Q.5 A digital computer has memory unit with 24 bits word. The instruction set consists of 150 different operations. All instructions have an operation code part and an address part. Each instruction is stored in one word of memory. How many bits are needed for the OPCODE and how many bits are left for the address of the instruction.

(a) 8, 16 (b) 16, 64
(c) 4, 8 (d) 8, 64

Q.6 An instruction is stored at location 300 with its address field. At location 301 the address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address matching the following addressing modes to their respective addresses.

A. Direct	1. 702
B. Immediate	2. 200
C. Relative	3. 400
D. Register indirect	4. 600
E. Index (R1 is index)	5. 301

(a) A3 B5 D2 E4 C1 (b) A3 B4 C1 D1 E5
(c) A5 B3 C2 D1 E4 (d) A4 B3 C1 D5 E2

Q.7 What is the most appropriate match for the items in the first column with the items in the second column:

Column 1:

X. Indirect addressing
Y. Indexed addressing
Z. Base register addressing

Column 2:

1. Array implementation
2. Writing relocatable code
3. Passing array as parameter

(a) X-3, Y-1, Z-2 (b) X-2, Y-3, Z-1
(c) X-3, Y-2, Z-1 (d) X-1, Y-3, Z-2

Q.8 In which of the following address mode, the content of the program counter is added to the address part of the instruction to get the effective address?
(a) Indexed addressing mode
(b) Implied addressing mode
(c) Relative addressing mode
(d) Register addressing mode

Q.9 In a certain processor, a 2 byte Jump instruction is encountered at memory address 3010H, the Jump instruction is in PC relative mode. The instruction is JMP – 7 where – 7 is signed byte. Determine the Branch Target Address
(a) 300B H (b) 3009 H
(c) 3003 H (d) 3007 H

Q.10 Processor *XYZ* supports only the immediate and the direct addressing modes. Which of the following programming language data structures cannot be implemented on this processors?
1. Pointers
2. Arrays
3. Records
(a) 1, 2 and 3 (b) 2 and 3
(c) 1 and 2 (d) Only 1

Q.11 Word 20 contains 40
Word 30 contains 50
Word 40 contains 60
Word 50 contains 70

Which of the following instructions loads 60 into the accumulator?
(a) Load immediate 20
(b) Load direct 30
(c) Load indirect 20
(d) Load indirect 30

Q.12 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	List-II
A. $A[1] = B[J]$;	1. Indirect addressing
B. while [*A++];	2. Indexed addressing
C. int temp = *x;	3. Auto-increment

Codes:

	A	B	C
(a)	3	2	1
(b)	1	3	2
(c)	2	3	1
(d)	1	2	3

Q.13 In immediate addressing mode, where is the operand placed?
(a) In memory
(b) In stack
(c) In CPU register
(d) In instruction after opcode

Q.14 A 4-byte long PC-relative branch instruction is fetched from memory address $(512)_{10}$ and while its execution, the branch is made to location $(885)_{10}$. What is unsigned displacement present in the instruction? (relative value) _____?

Q.15 A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____.

Q.16 The register which contains the data to be written into or read out of the addressed location is known as
(a) Memory address register
(b) Memory data register
(c) Program computer
(d) Index register

Q.17 In four-address instruction format, the number of bytes required to encode an instruction is (assume each address requires 24 bits and 1 byte is required for operation code)
(a) 9 (b) 13
(c) 14 (d) 12

Q.18 The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

MOVI Rs, 1;	Move immediate
LOAD Rd, 1000(Rs);	Load from memory
ADDI Rd, 1000;	Add immediate
STOREI 0(Rd), 20;	Store immediate

Which of the statements below is TRUE after the program is executed?
(a) memory location 1000 has value 20
(b) memory location 1020 has value 20
(c) memory location 1021 has value 20
(d) memory location 1001 has value 20

Q.19 A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

(a) 400 (b) 500
(c) 600 (d) 700

Q.20 Consider the following program segment:

	Instruction	Meaning	Size (words)
I_1	LOAD r_0, 500	$r_0 \leftarrow [500]$	2
I_2	MOV r_1, r_0	$r_0 \leftarrow r_0$	1
I_3	Add r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_4	Inc r_0	$r_0 \leftarrow r_0 + 1$	1
I_5	Inc r_1	$r_1 \leftarrow r_1 + 1$	1
I_6	Add r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_7	Store r_1, r_0	$M[(r_1)r_0]$	2
I_8	Halt	Stop	1

Assume that memory is word addressable with word size 32 bits. Program is loaded into memory location 3000 onwards. The value of PC at the end of execution of above program is _____.

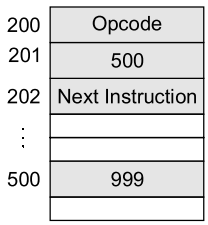
Q.21 A computer has 32 bit instruction and 9-bit address. If there are 400 two address instructions then how many one address instructions can be formulated?

(a) 2^{14} (b) $2^{32} - 200$
(c) $2^{14} - 400$ (d) $(2^{14} - 400) \times 2^9$

Q.22 In which addressing mode, the effective address of the operand is generated by adding a constant value to the content of a register?

(a) Absolute mode (b) Indirect mode
(c) Immediate mode (d) Index mode

Q.23 Consider a 16-bit processor in which the following one address Instruction appeals in main memory starting at location 200.



There is also a base register that contains the value 100.

Match **List-I** (Mode) with **List-II** (Effective Address) and select the correct answer using the codes given below the lists:

List-I	List-II
A. Immediate	1. 600
B. Direct	2. 999
C. Memory Indirect	3. 201
D. PC-relative	4. 500
E. Base-register	5. 702

Codes:

	A	B	C	D	E
(a)	3	5	2	4	1
(b)	4	5	2	1	3
(c)	3	4	2	5	1
(d)	3	4	5	1	2

Q.24 Most relevant addressing mode to write position independent code is

(a) direct (b) indirect
(c) relative (d) indexed mode

Q.25 Consider the following program segment. Here *R*1, *R*2 and *R*3 are the general purpose registers.

Instruction	Operation	Instruction Size (no. of words)
MOV *R*1, 3000	*R*1 ← *M*[3000]	2
Loop:		
MOV *R*2,(*R*1)	*R*2 ← *M*[*R*3]	1
ADD *R*2, *R*1	*R*2 ← *R*1 + *R*2	1
MOV (*R*3), *R*2	*M*(*R*3] ← *R*2	1
INC *R*3	*R*3 ← *R*3 + 1	1
DEC *R*1	*R*1 ← *R*1 – 1	1
BNZ LOOP	Branch on not zero	2
Halt	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register *R*3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 100. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

(a) 10 (b) 11
(c) 20 (d) 21

Q.26 Consider the hypothetical processor is support both 2 address instructions. It has 128 word memory. A 16-bit instruction is placed in the one memory word. If two 2-address instructions are already existed. How many one address instruction can be supported?

(a) 128 (b) 2
(c) 256 (d) 32

Q.64 Consider the following statements. Which of the following is correct for the computers that uses memory mapped I/O?

(a) The computer provides special instruction for manipulating I/O port.

(b) I/O ports are placed at address on bus and as accessed just like other memory location.

(c) To perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation.

(d) Ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.

Q.65 Consider a hypothetical system which has 32 bit instruction size and 8 bit address. If there are 180 2-address instructions and 400 one 1-address instruction then which of the following are correct?

(a) Total opcodes possible is 2^{12}.

(b) Number of 1-address instruction
$= (2^{16} - 180) \times 2^8$

(c) Number of zero-address instruction
$= ((2^{16} - 180) \times 2^8 - 400) \times 2^8$

(d) Number of zero-address instruction
$= (2^{16} - 180 \times 2^8 - 400) \times 2^8$

Q.66 Which of the following statement are correct?

(a) Address decoder is an essential part of I/O interface.

(b) Compared to RISC processor CISC processor contains large instruction set and less number of registers.

(c) Separate I/O address space does not necessarily mean that I/O address lines are physically separated.

(d) None of these

■■■■

Answers Machine Instructions and Addressing Modes

1.	(b)	**2.**	(c)	**3.**	(a)	**4.**	(c)	**5.**	(a)	**6.**	(a)	**7.**	(a)
8.	(c)	**9.**	(a)	**10.**	(c)	**11.**	(c)	**12.**	(c)	**13.**	(d)	**14.**	(369)
15.	(16383)	**16.**	(b)	**17.**	(b)	**18.**	(d)	**19.**	(c)	**20.**	(3009)	**21.**	(d)
22.	(d)	**23.**	(c)	**24.**	(c)	**25.**	(d)	**26.**	(c)	**27.**	(b)	**28.**	(c)
29.	(d)	**30.**	(b)	**31.**	(c)	**32.**	(b)	**33.**	(c)	**34.**	(c)	**35.**	(c)
36.	(369)	**37.**	(a)	**38.**	(c)	**39.**	(b)	**40.**	(a)	**41.**	(–128)	**42.**	(a)
43.	(a)	**44.**	(d)	**45.**	(a)	**46.**	(d)	**47.**	(16)	**48.**	(b)	**49.**	(c)
50.	(a)	**51.**	(92)	**52.**	(2032)	**53.**	(c)	**54.**	(a)	**55.**	(b)	**56.**	(c)
57.	(c)	**58.**	(2048)	**59.**	(d)	**60.**	(a)	**61.**	(a, b, d)	**62.**	(c)	**63.**	(b, c)
64.	(b)	**65.**	(b, c)	**66.**	(a, b, c)								

Explanations **Machine Instructions and Addressing Modes**

2. (c)

For making use of pointer in programs, indirect addressing mode is used.

Pointer stores the address of a variable and indirect addressing mode stores address of effective address the instruction.

Position independent code make use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.

Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

4. (c)

Memory size = 4 GB = 2^{32} B

Word size = 2 B

So, unique address = $\frac{2^{32}}{2^{1}} = 2^{31}$

Hence, atleast 31 bits are required.

5. (a)

Each instruction is stored in one word of memory.

Memory is word addressable and 1 word = 24 bits $\Rightarrow$ 3 bytes.

Total number bits = 24

The instruction set consists of 150 different operations. To generate 150 different operations we need minimum 8 bits are required.

OP code	Address
8	16

So, option (a) is correct.

6. (a)

For direct, EA = address field value in IR (instruction register) = 400

For immediate, actually no meaning of effective address. So, EA here will be just the address of the operand field which is otherwise address field = 301.

For relative addressing, we have EA = PC value (current) + Address field value

EA = 302 + 400 = 702

For register indirect, the EA is the content of the register, the register name being present in the address field of instruction.

So, EA = content of R1 = 200

For indexed mode = Base address + index register content

= 400 + 200 = 600

So, option (a) is correct.

8. (c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

So, option (c) is correct.

9. (a)

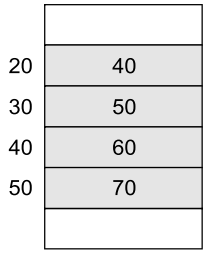
The Jump instruction is at address 3010 H and instruction is 2 bytes. Therefore, PC points to 3012 H on execution of this instruction.

Now Branch Target PC = PC + (–7)

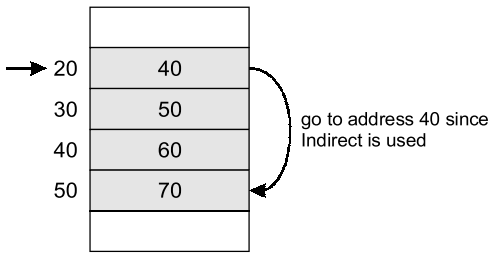
= 3012 H – 7 H = 300 BH

11. (c)

The given information can be understood as



Now load indirect 20 will load 60 into as follows



Hence (c) is correct option.

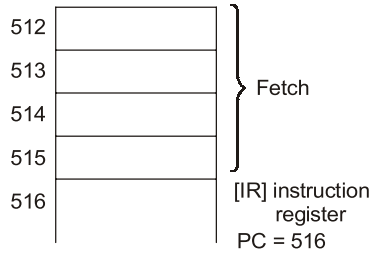
13. (d)

In immediate addressing mode, the operand is specified in the instruction itself.

For example: MOV R1, 12H is the immediate AM with 12 is operand.

14. (369)

4 byte instruction storage



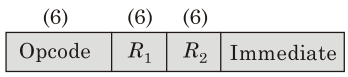
Effective address = PC + Relative value

Relative value = EA – PC

= 885 – 516 = (369)10

So, answer is 369.

15. (16383)



32 – (6 + 6 + 6) = 14 bits for immediate field

$\Rightarrow 2^{14} - 1 = 16383$ maximum possible value of immediate operand.

16. (b)

MDR register needed to read or written data into or onto memory location.

17. (b)

Four address instruction format:

Opcode	A_1	A_2	A_3	A_4
8 bits	24 bits	24 bits	24 bits	24 bits

So total bits needed = (24 bits × 4) + 8 bits

= 96 + 8 bits = 104 bits

So number of bytes = $\frac{104}{8}$ byte = 13 bytes

18. (d)

$M[1000] = 18,\ M[1001] = 1,\ M[1020] = 16$

MOV I R_S, 1	$R_S = 1$
LOAD R_D, 1000 (R_S)	$R_D \leftarrow M[1000+[R_S]]$
	$R_D \leftarrow M[1000+1] = M[1001]$
	$R_D \leftarrow 1$
ADD I R_d, 1000	$R_d \leftarrow R_d + 1000 = 1+1000 = 1001$
STORE I 0(R_d), 20	$M[0+R_d] = 20$
	$M[R_d] = 20$
	$M[1001] = 20$

19. (c)

As the instruction are 24 bit or 3 bytes, the value of program counter at any time should be multiple of 3 starting from 300 like 300, 303, 306 ... from options, '600' is multiple of 3 or is included in above series.

20. (3009)

Word addressable storage

3000 – 3001

3002

3003

3004

3005

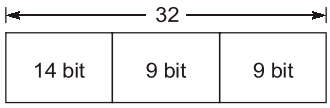
3006

3007-3008

3009

Valid program counter value after program is 3009.

21. (d)



2^{14} two address instructions are possible. Here, 400 two addresses are needed.

So, $(2^{14} - 400)$ opcode are free.

We can store $(2^{14} - 400) \times 2^9$ one address instructions.

22. (d)

Index addressing mode:

Effective address = [Base address + Displacement]

23. (c)

PC-relative → PC + 500 = 202 + 500 = 702

Base-register→ 100 + 500 = 600

24. (c)

Relative mode always find based on PC value.

25. (d)

	MOV $R1$, 3000	$R1 \leftarrow M[3000]$	1 memory reference
Loop:	MOV $R2$, $R1$	$R2 \leftarrow M[R3]$	1 memory reference
	ADD $R2$, $R1$	$R2 \leftarrow R1 + R2$	
	MOV ($R3$), $R2$	$M[R3] \leftarrow R2$	1 memory reference
	INC $R3$	$R3 \leftarrow R3 + 1$	
	DEC $R1$	$R1 \leftarrow R1 - 1$	
	BNZ loop		
	HALT		

Total memory references = 2 × Number of times loop runs + 1 = 2 × 10 + 1 = 21