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ELECTRICAL ENGINEERING

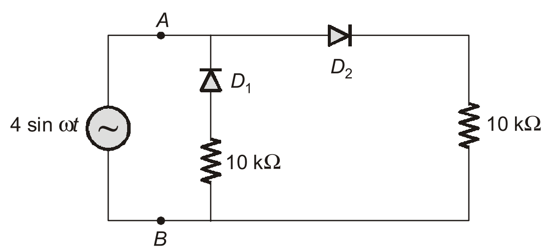
CONVENTIONAL Practice Sets

CONTENTS

ANALOG ELECTRONICS

CHAPTER 1 Diode Circuits

Q.1 A voltage source $V_{AB} = 4 \sin \omega t$, is applied across the terminals A and B of the circuit. The diodes are assumed to be ideal. Find the impedance offered by the circuit across the terminals A and B in kilo ohm.

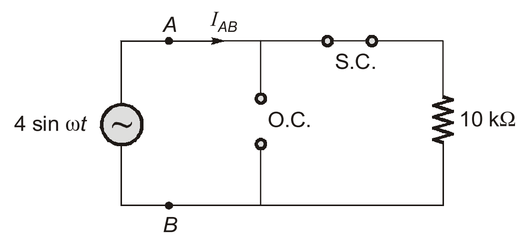


Solution:

In +ve half cycle D_1 – off (R.B.)

D_2 – on (F.B.)

∴ Equivalent circuit will be



$$V_{AB} = 4 \sin\omega t$$

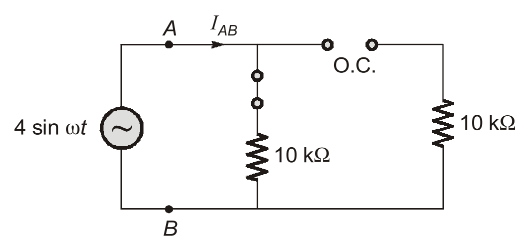
$$I_{AB} = \frac{V_{AB}}{10\,\text{k}\Omega}$$

∴ $$R_i = \frac{V_{AB}}{I_{AB}} = 10\,\text{k}\Omega$$

For –ve half cycle,

D_1 on, D_2 off

Equivalent circuit,

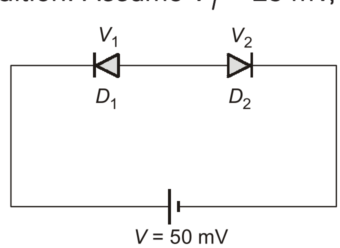


$$V_{AB} = 4 \sin\omega t$$

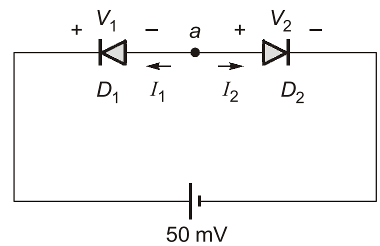
$$I_{AB} = \frac{4 \sin\omega t}{10\,\text{k}\Omega}$$

∴ $$\frac{V_{AB}}{I_{AB}} = R_i = 10\,\text{k}\Omega$$

Q.2 Two ideal and identical junction diodes are connected as shown in Figure. If the current through the reverse-biased diode is I_0 and is constant, explain the circuit operation when both the diodes are connected in forward-biased condition. Assume $V_T = 25$ mV, $V_\gamma = 0.7$ V and $\eta = 1$ for the diodes.



Solution:



Case 1: Diode D_1 is in reverse bias where as D_2 is forward biased.

At Node '*a*'

$$I_1 + I_2 = 0$$

$$I_1 = -I_2$$

$$I_S\left(e^{-\frac{V_1}{\eta V_T}} - 1\right) = -I_S\left(e^{\frac{+V_2}{\eta V_T}} - 1\right)$$

$$e^{-\frac{V_1}{\eta V_T}} + e^{\frac{V_2}{\eta V_T}} = 2$$

Also,

$$V_2 = 50 - V_1$$

$\therefore$

$$e^{-\frac{V_1}{\eta V_T}} + e^{\frac{50 - V_1}{\eta V_T}} = 2$$

$$e^{-\frac{V_1}{\eta V_T}}\left[1 + e^{\frac{50}{\eta V_T}}\right] = 2$$

$$e^{-\frac{V_1}{V_T}} = \frac{2}{1+e^2} \qquad (\eta = 1,\ V_T = 25 \text{ mV})$$

$$e^{-\frac{V_1}{V_T}} = \frac{2}{3.39} = 0.24$$

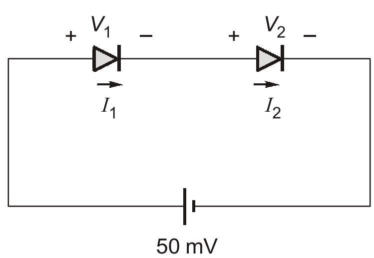
Putting in I_1,

$$I_1 = I_0 = I_S\left[e^{-\frac{V_1}{V_T}} - 1\right]$$

$$I_1 = I_0 = -0.76\, I_s$$

–ve sign denotes that direction of current will be opposite to the assumed direction.

Case 2: Both the diodes are forward biased.



As both diodes are ideal and identical hence voltage drop across both diodes will be same.

$\therefore$

$$V_1 = V_2 = 25 \text{ mV}$$

Now,

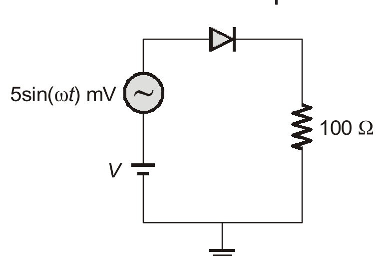
$$I_1 = I_2 = I_s\left(e^{\frac{V_1}{V_T}} - 1\right) = I_s\left(e^{\frac{25}{25}} - 1\right) = 1.72\, I_s$$

$$\frac{I_1}{I_0} = \frac{1.72\, I_s}{0.76\, I_s} = 2.26$$

$\therefore$

$$I_1 = 2.26 I_0$$

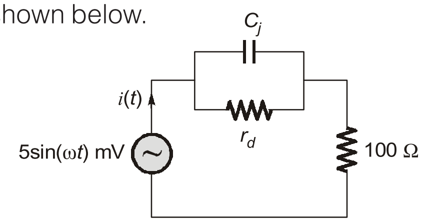
Q.3 A DC current of 26 μA flows through the circuit shown. The diode in the circuit is forward biased and it has an ideality factor of one. At the quiescent point, the diode has a junction capacitance of 0.5 nF. Its neutral region resistances can be neglected. Assume that the room temperature thermal equivalent voltage is 26 mV.



For $\omega = 2 \times 10^6$ rad/s, the amplitude of the small-signal component of diode current.

Solution:

The small-signal equivalent model of the given circuit can be drawn as shown below.



Given that,

$$\omega = 2 \times 10^6 \text{ rad/sec}$$
$$C_j = 0.5 \text{ nF}$$
$$I_{DC} = 26\ \mu\text{A}$$
$$V_T = 26 \text{ mV}$$
$$\eta = 1$$

Since, small signal incremental diode resistance, $r_d = \dfrac{\eta V_T}{I_{DC}} = \dfrac{26 \text{ mV}}{26\ \mu\text{A}} = 1\text{k}\Omega$

and impedance due to junction capacitance, $\dfrac{1}{\omega C_j} = \dfrac{1}{2 \times 10^6 \times 0.5 \times 10^{-9}}\ \Omega = 1\text{k}\Omega$

So, total impedance of the circuit will be,

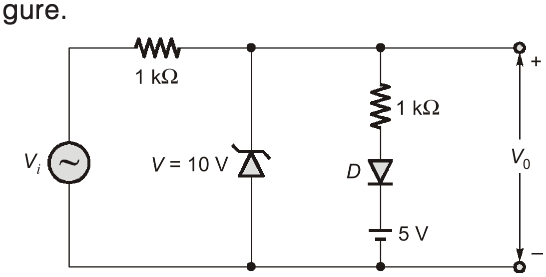
$$Z = \left(r_d \Big\| \frac{1}{j\omega C_j} \right) + 100\ \Omega$$

$$\left(r_d \Big\| \frac{1}{j\omega C_j} \right) = \frac{(1000)(-j1000)}{1000 - j1000}\ \Omega = \frac{-j(1+j)}{2}\ \text{k}\Omega = \frac{1}{2}(1-j)\ \text{k}\Omega = (500 - j500)\ \Omega$$

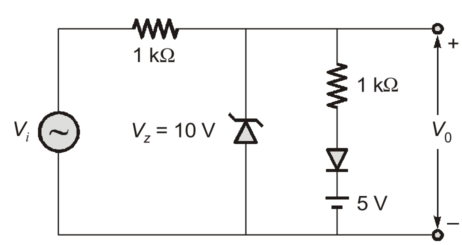
$\therefore$

$$Z = 600 - j500\ \Omega$$
$$|Z| = 100\sqrt{36+25} = 100\sqrt{61}\ \Omega$$
$$I_m = \frac{V_m}{|Z|} = \frac{5 \text{ mV}}{100\sqrt{61}\ \Omega} = \frac{50}{\sqrt{61}}\ \mu\text{A} = 6.40\ \mu\text{A}$$

Q4 Assuming forward voltage drop across diodes to be 0.7 V, draw the transfer characteristic of the clipper circuit shown in figure.

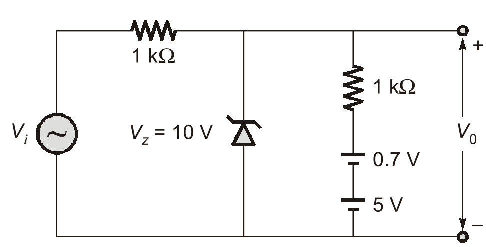


Solution:



When V_i is +ve and $V_i > 5.7$ V

Assume diode is conducting,



Assume the zener diode is reverse biased and having voltage less than breakdown voltage

$$V_i - I(1\text{ k}\Omega) - I(1\text{ k}\Omega) - 0.7 - 5 = 0$$

$$V_i - I(2\text{ k}\Omega) - 5.7 = 0$$

$$I(2\text{ k}\Omega) = V_i - 5.7$$

$$I = \left(\frac{V_i - 5.7}{2\text{ k}\Omega}\right)$$

$$V_0 = 5.7 + 1 \times I$$

$$= 5.7 + \left(\frac{V_i - 5.7}{2}\right) = \left(\frac{5.7 + V_i}{2}\right)$$

When, $V_i < 5.7$ V

$$V_0 = V_i$$

If, $5.7 < V_i < 14.3$ (∵ Diode is in off state)

$$V_0 = \left(\frac{5.7 + V_i}{2}\right)$$

Diode conducts and zener diode is reverse biased,

When, $V_i > 14.3$ V

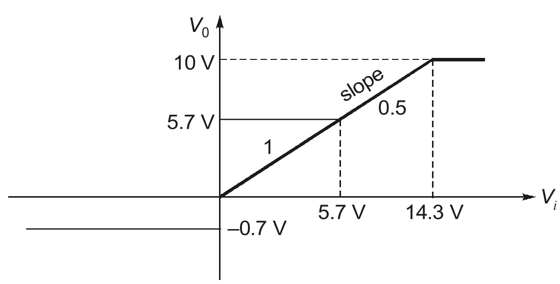
⇒ $V_0 = 10$ volts

Breakdown occurs in zener diode.

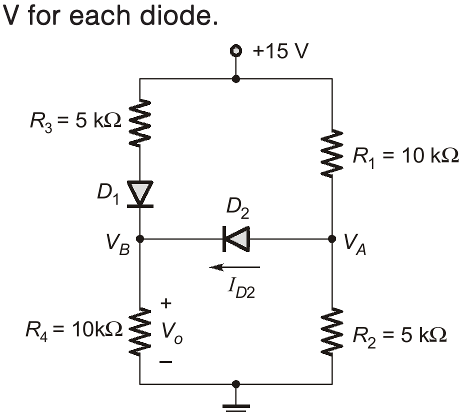
When, $V_i < 0$ V

$$V_0 = -0.7 \text{ V}$$

Transfer characteristics:



Q.5 Determine the current I_{D2} and the voltage V_o in the multidiode circuit shown in the figure below. Assume that, cut-in voltage $V_\gamma = 0.7$ V for each diode.



Solution:

To begin, initially assume that, both the diodes D_1 and D_2 are in their conducting state.

By applying KCL at A and B nodes, we have

$$\frac{15 - V_A}{10} = I_{D2} + \frac{V_A}{5} \quad \text{...(i)}$$

and $$\frac{15-(V_B+0.7)}{5}+I_{D2} = \frac{V_B}{10} \quad \text{...(ii)}$$

We note that $V_B = V_A - 0.7$. Combining the two equations and eliminating I_{D2}, we find

$$V_A = 7.62\text{ V} \quad \text{and} \quad V_B = 6.92\text{ V}$$

From equation (i) above, we obtain

$$\frac{15-7.62}{10} = I_{D2}+\frac{7.62}{5} \Rightarrow I_{D2} = -0.786\text{ mA}$$

We assumed that D_2 was ON, so a negative current is inconsistent with that initial assumption.

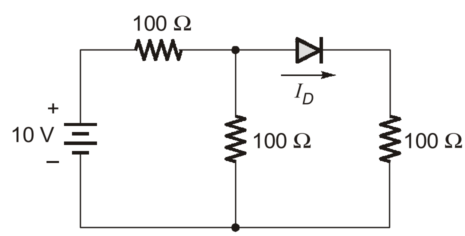
Now assume that diode D_2 is OFF and D_1 is ON. To find the node voltages, we can simply use voltage divider principle as

$$V_A = \left(\frac{5}{5+10}\right)(15) = 5\text{ V}$$

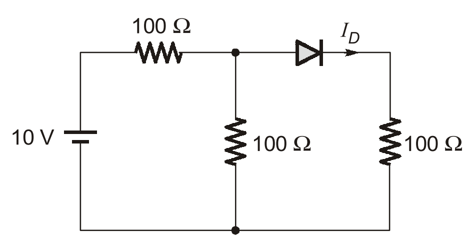
and $$V_B = V_o = \left(\frac{10}{10+5}\right)(15-0.7) = 9.53\text{ V}$$

These voltages show that diode D_2 is indeed reverse biased so that $I_{D2} = 0$.

Q.6 **Find the diode current I_D in the circuit shown below when the diode has cut in voltage, $V_\gamma = 0.7$ V and forward resistance, $R_f = 25\ \Omega$.**

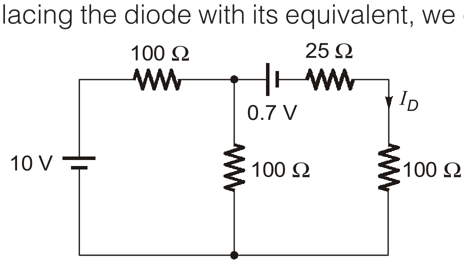


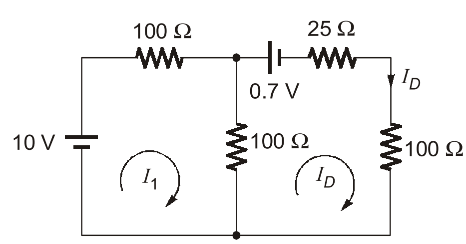
Solution:



Given : Diode cut-in voltage = 0.7 V and diode forward resistance = 25 Ω

Replacing the diode with its equivalent, we get,





Using KVL, $$10-100I_1-100(I_1-I_D) = 0 \quad \text{...(i)}$$

$$-0.7-125I_D+100(I_1-I_D) = 0 \quad \text{...(ii)}$$

Solving equation (i) and (ii)

$$10-200I_1-100I_D = 0 \quad \text{...(iii)}$$

$$-0.7-225I_D+100I_1 = 0 \quad \text{...(iv)}$$

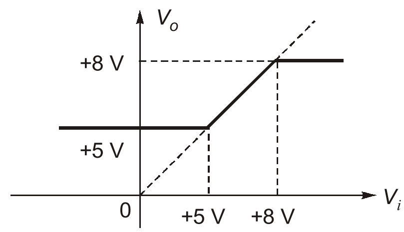
Multiplying equation (iv) by 2 and adding, we get

$$10 - 1.4 - 450I_D - 100I_D = 0$$

$$8.6 = 550I_D$$

$$\therefore \quad I_D = \frac{8.6}{550} = 15.63 \text{ mA}$$

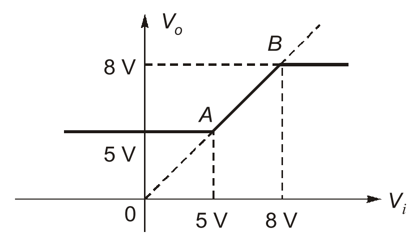
Q.7 The ideal transfer characteristic of a particular circuit is given in figure. Design the circuit. Draw the output waveform with proper explanation, if $V_i = 10 \sin \omega t$.



Solution:

Slope of the curve between A and B is

$$m = \frac{(8-5)}{(8-5)} = 1$$

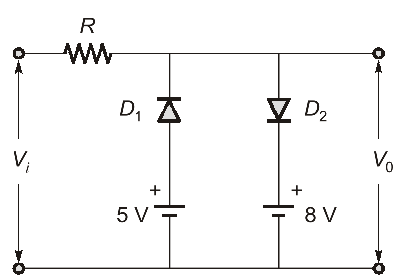


The circuit diagram for the above input-output (transfer) characteristic is a two-level clipper as shown below.

Cut in voltages of diodes are zero.

For $V_i < 5$ V $\rightarrow$ diode D_1 will be on and D_2 will be off

and $\boxed{V_0 = 5\text{ V}}$



For $V_i > 8$ V $\rightarrow$ diode D_1 will be off and diode D_2 will be on

and $\boxed{V_0 = 8\text{ V}}$

For $5 < V_i < 8$ V $\rightarrow$ both the diodes will be off

and $\boxed{V_0 = V_i}$

Given that $V_i = 10 \sin \omega t$

or $V_i = 10 \sin\theta$ $(\omega t = \theta)$

For $V_i < 5$; $10\sin\theta < 5 \Rightarrow 0 < \theta < 30°$ and $150° < \theta < 360°$

$V_o = 5$ V

For $V_i > 8$ V; $10\sin\theta > 8 \Rightarrow 53.13° < \theta < 126.869°$

$V_o = 8$ V

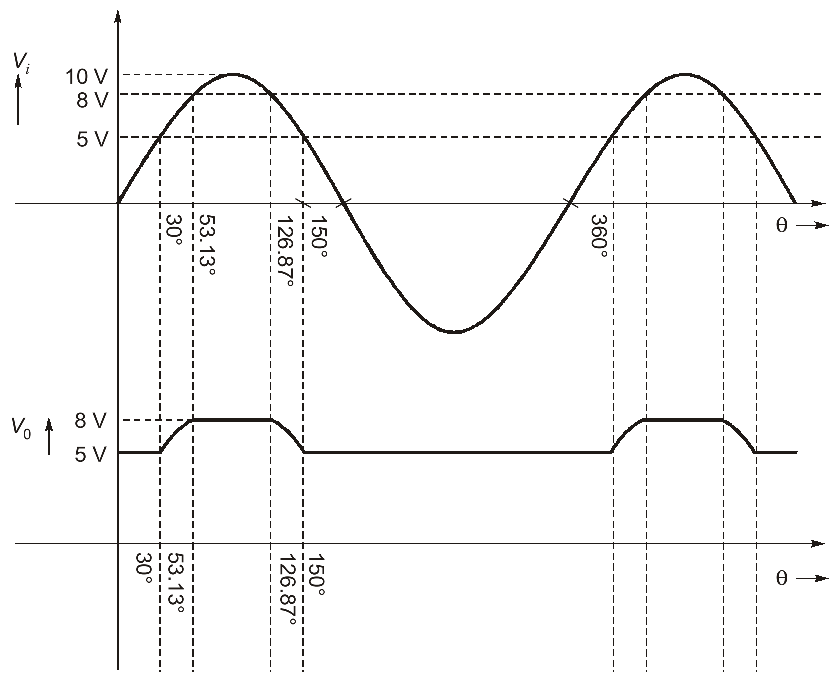
For $5 < V_i < 8$ V; $30° < \theta < 53.13°$ and $126.87° < \theta < 150°$

$V_o = V_i$

The required voltage-current characteristics can be written as

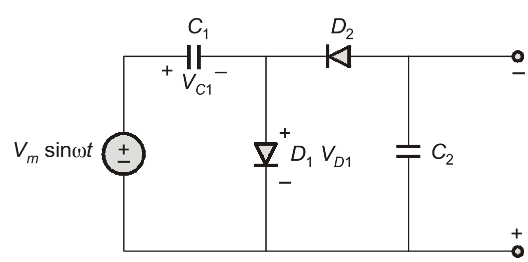
$$V_o = \begin{cases} 5\text{ V} & ; \quad V_i < 5\text{ V} \\ V_i & ; \quad 5\text{ V} < V_i < 8\text{ V} \\ 8\text{ V} & ; \quad V_i > 8\text{ V} \end{cases}$$

Now output waveform will be



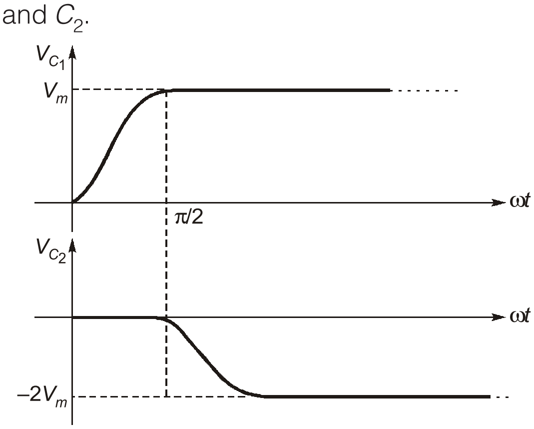
Q.8 Draw the neat circuit of a voltage doubler. Explain its operation. Draw the waveforms for the voltages across the two capacitors.

Solution:



Voltage follower circuit

The figure shows a circuit-composed of two sections in cascade, a clamp circuit formed by C_1 and D_1 and peak rectifier formed by D_2 and C_2.



When excited by a sinusoidal of amplitude V_m the clamping section provides the waveform shown. Assuming ideal diodes, while the positive peaks are damped to 0 V, the negative peak reaches $-2V_m$. In response to this wave form, the peak-detector section provides, across capacitor C_2 a negative dc voltage of magnitude $2V_m$. Because the output voltage is double the input peak, the circuit is known as a voltage doubler.

Q.9 For the circuit shown in the figure (a), the input voltage waveform V_i is shown in figure (b). Assume that the RC time constant is large and the cut-in voltage of diode $V_\gamma = 0$ V. Determine the output voltage waveform.

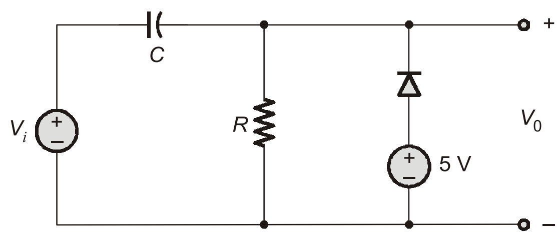


Fig. (a)

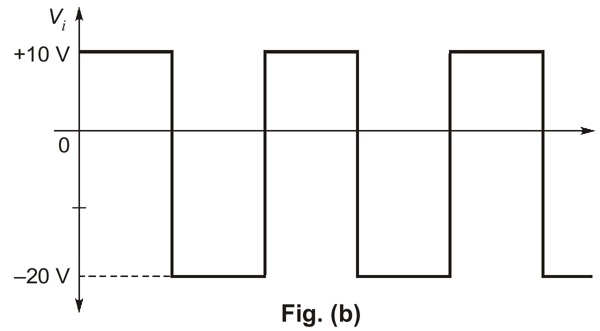
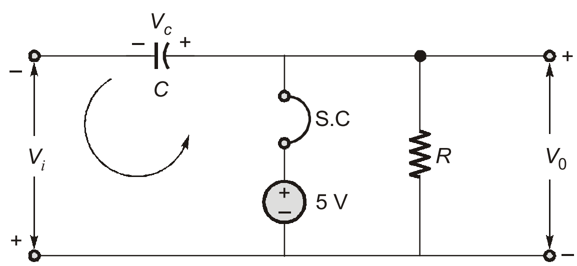


Fig. (b)

Solution:

Considering first the negative half cycle of the input signal V_i, the diode will be forward biased and acts as a short-circuit. The equivalent circuit can be drawn as:



The capacitor charges and the voltage across the capacitor can be calculated using KVL as below:

$$-V_i - 5 + V_c = 0$$

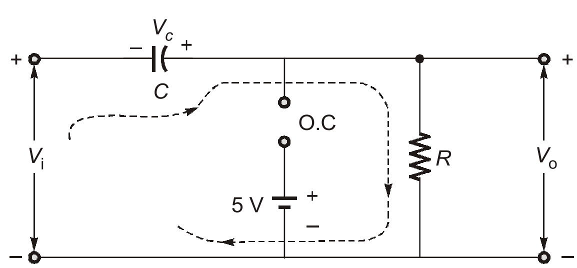
or $\quad V_c = V_i + 5 \quad$ or $\quad V_c = 20 + 5$

$\therefore \quad V_c = 25$ volt

During this period, diode is short circuited, hence battery voltage (+5 V) appears across the output,

$$V_0 = 5 \text{ V}$$

Now, we have to consider the positive half cycle of the input voltage where the diode '*D*' is reversed biased and so it acts as open circuit. The capacitor voltage 'V_c' (due to charging in the previous negative half cycle duration) comes in the series as shown in the circuit given below:



$$-V_i - V_c + V_0 = 0$$

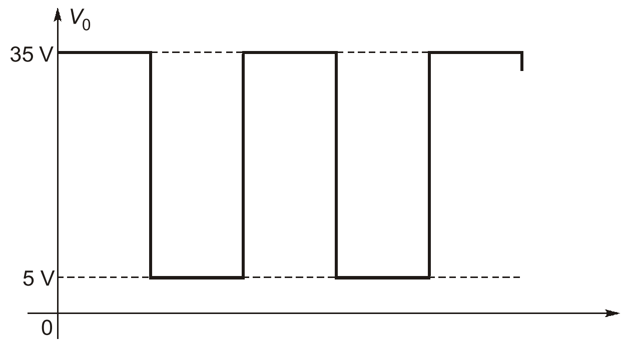
or $\quad V_0 = V_i + V_c \quad$ or $\quad V_0 = 10 + 25$

$\therefore \quad V_0 = 35$ V

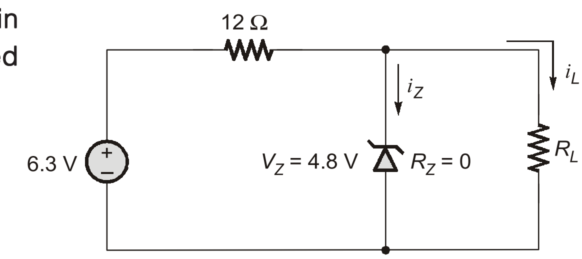
Since the time constant *RC* is very large, the capacitor voltage negligibly discharges through *R* and the capacitor voltage can be treated as constant at $V_C = 25$ V. The diode, therefore, remains reverse-biased during both positive and negative input cycle.

Hence, $\quad V_o = V_i + V_c = V_i + 25$

So, the output waveform (V_0) is shown below:

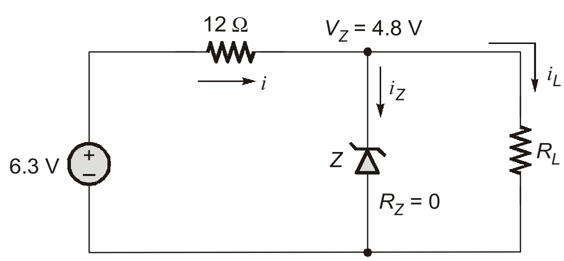


Q.10 In the Zener diode voltage regulator circuit as shown in the figure below, the Zener diode current is to be limited to the range, $5 \le i_Z \le 100$ mA.
Determine:
(a) the range of the possible load currents.
(b) the range of the possible load resistances.
(c) power rating required for the load resistor.



Solution:

(a)



The total current (i) = $i_Z + i_L$

or $$\frac{6.3-4.8}{12} = i_Z + i_L$$

or $$i_Z + i_L = 0.125 \text{ A} \approx 125 \text{ mA} \quad \text{...(i)}$$

Also, $$i_L = (125 - i_Z) \text{ mA} \quad \text{...(ii)}$$

As we are given that, the Zener diode current varies as,

$$5 \le i_Z \le 100 \text{ mA}$$

$$\Rightarrow \quad 5 \le (125 - i_L) \le 100 \text{ mA}$$

$$\Rightarrow \quad 5 - 125 \le -i_L \le (100 - 125) \text{ mA}$$

$$\Rightarrow \quad -120 \le -i_L \le -25 \text{ mA}$$

$$120 \ge i_L \ge 25 \text{ mA}$$

So, the possible range of the load current 'i_L' is as, $25 \le i_L \le 120$ mA

(b) Load current (i_L) = V_Z / R_L

$$\Rightarrow \quad R_L = \frac{V_Z}{i_L} = \frac{4.8\text{ V}}{i_L}$$

when, i_L = 25 mA then,

$$R_L = \frac{4.8}{25} = 192\,\Omega$$

and when i_L = 120 mA then,

$$R_L = \frac{4.8}{120} = 40\,\Omega$$

So, the range of the possible load resistance (R_L) is given as,

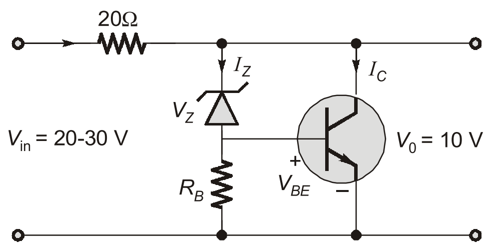
$$40 \le R_L \le 192\ \Omega$$

(c) Power rating required for the load resistor is given as,

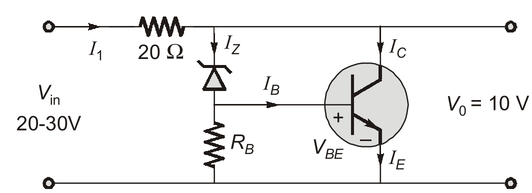
$$P_{Zm} = i_{L\,max} \times V_Z = 120 \text{ mA} \times 4.8 \text{ V}$$

$$\therefore \quad P_{Zm} = 576 \text{ mWatt}$$

Q.11 The transistor shunt regulator shown in the figure has a regulated output voltage of 10 V, when the input varies from 20 V to 30 V. The relevant parameters for the Zener diode and the transistor are: $V_Z = 9.5$, $V_{BE} = 0.5$ V, $\beta = 99$. Neglect the current through R_B. Find the maximum power dissipated in the Zener diode (P_Z) and the transistor (P_T).



Solution:



$$I_{1max} = \frac{V_{in\,max} - V_o}{20}$$

$$I_{1\,max} = \frac{30-10}{20} = 1 \text{ A}$$

$$I_E = I_B + I_C$$

$$I_E = I_C + I_Z \qquad [\because\ I_B = I_Z \text{ (as no current flows in } R_B)] \qquad \text{...(i)}$$

$$\beta = \frac{I_C}{I_B} = \frac{I_C}{I_Z}$$

$$\Rightarrow \quad I_C = \beta I_Z$$

From (i), $I_E = \beta I_Z + I_Z = (99 + 1)I_Z$

$$I_E = 100\,I_Z$$

$$I_1 = I_E = 100\,I_Z$$

$$I_Z = \frac{I_1}{100} = \frac{1}{100} = 0.01 \text{ A}$$

$$P_Z = V_Z I_Z = 9.5 \times 0.01 = 95 \text{ mW}$$

$$I_C = 99\,I_Z = 99 \times 0.01 = 0.99 \text{ A}$$

$$P_C = V_{CE} I_C = 10 \times 0.99 = 9.9 \text{ W}$$

Q.12 Answer the following with respect to the circuit shown:

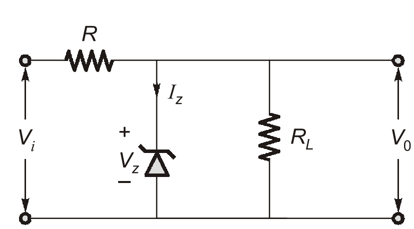
(i) Why is it called a 'shunt regulator'?

(ii) Which is the regulating element?

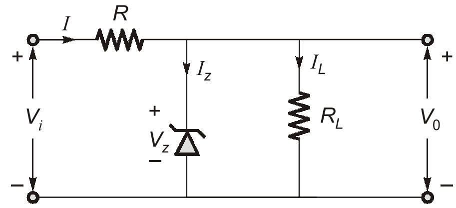
(iii) Draw the *v-i* characteristic of the regulating element.

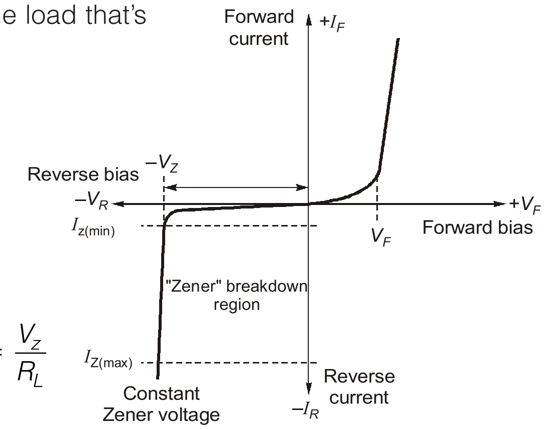
(iv) Mark the portion of the curve used for regulation.

(v) Show the range of current over which regulator will operate satisfactorily.



Solution:





- The control element (Zener diode) is in parallel with the load that's why it is called a shunt regulator.
- The regulating element is Zener diode.
- For fixed values of R_L, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage,

$$V_{i,\,\text{min}} = \frac{(R+R_L)V_Z}{R_L}$$

$$\therefore \qquad I_{\text{max}} = I_Z + I_L\,; \qquad \text{where,} \quad I_L = \frac{V_Z}{R_L}$$

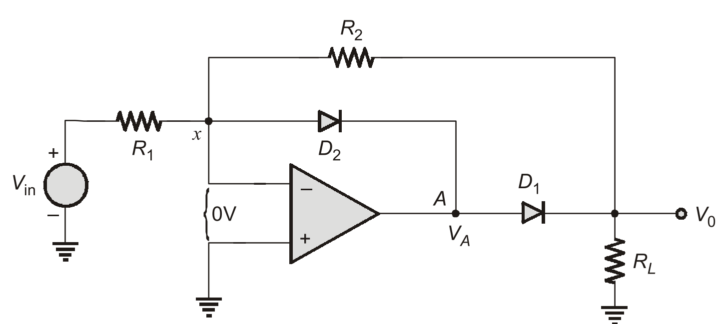
The maximum value of V_i

$$V_{i\,\text{max}} = I_{\text{max}} R + V_Z$$

Q.13 **Why do we use precision rectifiers? Draw the circuit diagram and explain the operation of an inverting half-wave precision rectifier.**

Solution:

- The major limitation with the silicon rectifiers is that, it cannot rectify an AC signal (V_{in}), whose magnitude is less than the forward voltage drops of a diode (V_D), which is typically 0.7 V.
- To remove this defect, precision rectifiers are used. An inverting half wave precision rectifier utilizes two diodes D_1 and D_2 and one op-amp as shown in the figure below. Using the precision rectifier, voltages in mV range can be rectified.

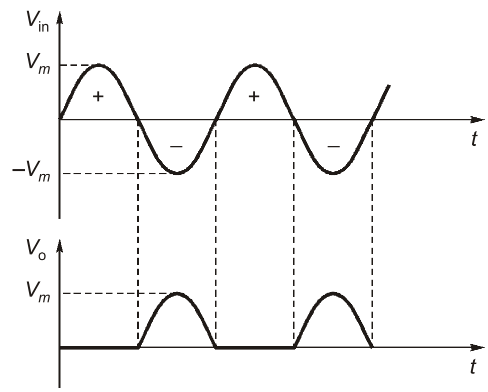


Case-1

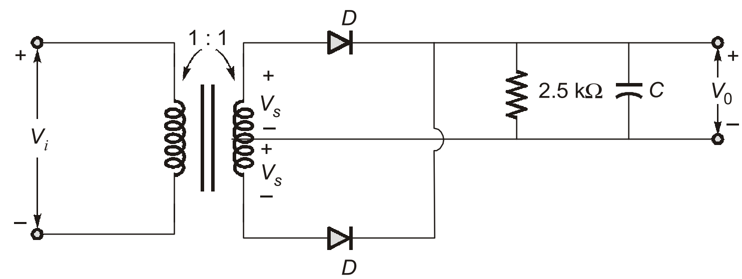
When V_{in} goes positive ($V_{\text{in}} > 0$) or during positive half cycle, the op-amp's output (V_A) becomes negative, which turns ON diode and as a result the negative feedback is established. As the non-inverting terminal of op-amp is at ground, the node (x) is virtual ground, therefore V_A is clamped at $-V_{D_2}$. As a result diode D_1 does not conduct and no current flows in the feedback resistor R_2, and so causes the rectifier output zero ($V_{\text{out}} = 0$). Thus when $V_{\text{in}} > 0$, $V_{\text{out}} = 0$.

Case-2

When $V_{\text{in}} < 0$ or during negative half cycle, the op-amp's output (V_A) becomes positive causing diode D_2 to turn OFF and diode D_1 is turned ON. The circuit behaves as an inverting amplifier. If $R_2 = R_1$ then $V_{\text{out}} = -V_{\text{in}}$ or V_{out} is out of phase with input. For a pure sinusoidal input the resulting output is shown below:



Q.14 Consider a Full Wave Rectifier (FWR) circuit shown below:



If V_i = 120 sin(2π 60)t, the diode cut-in voltage is 0.7 V and the output voltage cannot be dropped below 100 volt. Then calculate the required value of the capacitor 'C'?

Solution:

For a Full Wave Rectifier, it has been given that,

$$V_i = V_s = 120\sin(2\pi\,60)t \qquad \text{...(i)}$$

Here, $V_{i,\max} = 120$ volt

and frequency (f) = 60 Hz

We also know that in a FWR,

Frequency of output voltage, $f_{out} = 2f$; So time period of rectified V_o

$$T_1 = T_2 = \frac{T}{2} = \frac{1}{2f}$$

where, 'T' is the time period and the ripple voltage (V_{rip}) is related with peak voltage (V_p) as,

$$V_{rip} \approx V_p \cdot \frac{T_1}{CR}$$

$$\Rightarrow \quad V_{rip} \approx \frac{V_p}{2fRC} \qquad \text{...(ii)}$$

we know that,

Peak voltage across capacitor (V_p) = ($V_{imax} - V_\gamma$)

$$\therefore \quad V_p = (120 - 0.7) = 119.3 \text{ V}$$

and the ripple voltage (V_{rip}) may be defined as,

$$V_{rip} = (V_p - 100) = (119.3 - 100) \text{ V}$$

$$\therefore \quad V_{rip} = 19.3 \text{ volt}$$

Now from equation (ii) we obtained the value of 'C' by putting the values of V_p, V_{rip}, R and f as,

$$19.3 = \frac{119.3}{2 \times 60 \times 2.5 \times 10^3 \times C}$$

$$C = \frac{119.3}{5 \times 60 \times 10^3 \times 19.3} = 20.6\ \mu\text{F}$$