Electronics Engineering

Computer Organization and Architecture

Comprehensive Theory

with Solved Examples and Practice Questions

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CHAPTER 1

Computer Organization

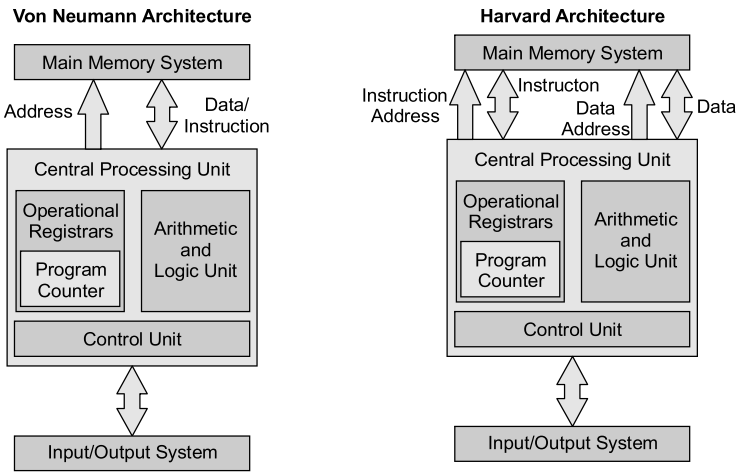
1.1 Computer Architecture Vs Computer Organization

Architecture and organization are independent; you can change the organization of a computer without changing its architecture.

1. The architecture indicates its hardware whereas the organization reveals its performance.
2. For designing a computer, its architecture is fixed first and then its organization is decided.

Computer Organization	Computer Architecture
• Computer organization deals with structural relationships that are not visible to the programmer (like clock frequency or the size of the physical memory).	• Computer architecture deals with the functional behavior of a computer system as viewed by a programmer (like the size of a data type – 32 bits to an integer).
• A computer's organization expresses the realization of the architecture.	• A computer's architecture is its abstract model and is the programmer's view in terms of instructions, addressing modes and registers.
• Organization describes how it does it.	• Architecture describes what the computer does.

Von Neumann Architecture Vs Harvard Architecture



1.2 Evolution of Digital Computers

First generation: Vacuum tube computers (1945~1953)

- Program and data reside in the same memory (stored program concepts: John von Neumann)
- Vacuum tubes were used to implement the functions (ALU & CU design)
- Magnetic core and magnetic tape storage devices are used.
- Using electronic vacuum tubes, as the switching components.
- Assembly level language is used

Second generation: Transistorized computers (1954~1965)

- Transistor were used to design ALU & CU
- High Level Language is used (FORTRAN)
- To convert HLL to MLL compiler were used
- Separate I/O processor were developed to operate in parallel with CPU, thus improving the performance
- Invention of the transistor which was faster, smaller and required considerably less power to operate

Third generation: Integrated circuit computers (1965~1980)

- IC technology improved
- Improved IC technology helped in designing low cost, high speed processor and memory modules
- Multiprogramming, pipelining concepts were incorporated
- DOS allowed efficient and coordinate operation of computer system with multiple users
- Cache and virtual memory concepts were developed
- More than one circuit on a single silicon chip became available.

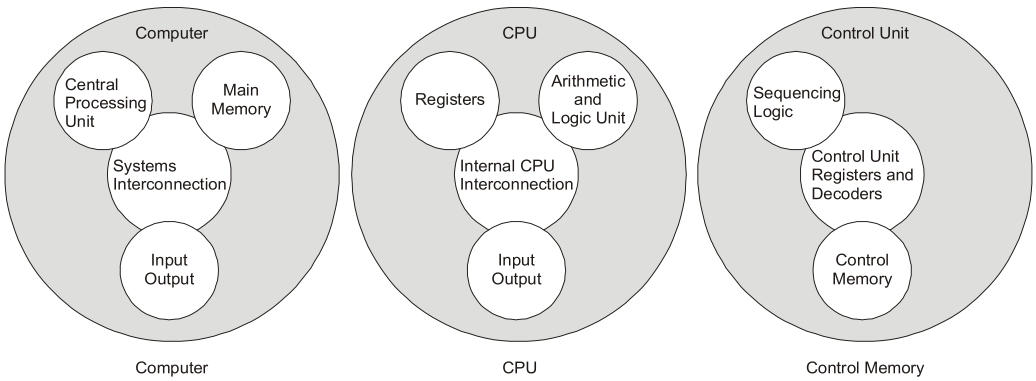
Fourth generation: Very large scale integrated (VLSI) computers (1980~2000)

- CPU termed as microprocessor
- INTEL, MOTOROLA, TEXAS, NATIONAL semiconductors started developing microprocessor
- Workstations, microprocessor (PC) & Notebook computers were developed
- Interconnection of different computer for better communication LAN, MAN, WAN
- Computational speed increased by 1000 times
- Specialized processors like Digital Signal Processor were also developed.

Fifth generation: System-on-chip (SOC) computers (2000~)

- E-Commerce, E- banking, home office
- ARM, AMD, INTEL, MOTOROLA
- High speed processor - GHz speed
- Because of submicron IC technology, more features were added in small size.

1.3 Components of Computer Structure



Computer Structure vs CPU Structure vs Control Unit

1. **Input Unit**: Computers can understand only machine language. Therefore for converting data from human language to machine language we use some special peripheral devices which are called input device.
   Examples: Keyboard, Mouse, Joystick, etc.
2. **Output Unit:** After passing instructions for solving particular problem, the results came out from computer comes in machine language and this is very difficult to convert that results into human language. There are several peripheral devices which help us to convert the machine language data into human acceptable data. These devices are called output devices.
   Examples: Monitor, Printer, LCD, LED etc.
3. **Memory Unit:** Which is used to store data in computer.
   Memory unit performs the following functions
   (a) Stores data and instructions required for processing.
   (b) Stores the intermediate results obtain during processing.
   (c) Stores final results before sending it to output unit.

   Two class of storage units: (i) Primary Memory (ii) Secondary Memory
   Two types of primary memory are RAM (Random Access Memory) and ROM (Read Only Memory). RAM is used to store data temporarily during the program execution. ROM is used to store data and program which is not going to change.
   Secondary Memory is used for bulk storage or mass storage to store data permanently.
4. **CPU:** It is main unit of the computer system. It is responsible for carrying out computational task. The major structural components of a CPU are:
   (a) *Control Unit (CU):* Controls the operation of the CPU and hence the computer.
   (b) *Arithmetic and Logic Unit (ALU):* Performs computer's data processing functions.
   (c) *Register:* Provides storage internal to the CPU.
   (d) *CPU Interconnection:* communication among the control unit, ALU, and register.

1.4 CISC and RISC Architectures

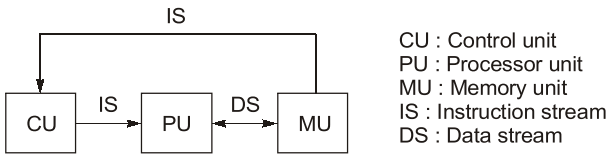
CISC (Complex Instruction Set Computers)	RISC (Reduced Instruction Set Computers)
• Large instruction set	• Compact instruction set
• Instruction formats are of different lengths	• Instruction formats are all of the same length
• Instructions perform both elementary and complex operations	• Instructions perform elementary operations
• Control unit is micro□]rogrammed	• Control unit is simple and hardwired
• Not pipelined or less pipelined	• Pipelined
• Single register set	• Multiple register set
• Numerous memory addressing options for operands	• Compiler and IC developed simultaneously
• Emphasis on hardware	• Emphasis on software
• Includes multi-clock complex instructions	• Single-clock, reduced instruction only
• Memory-to-memory: "LOAD" and "STORE" incorporated in instructions	• Register to register: "LOAD" and "STORE" are independent instructions
• Small code sizes, high cycles per second	• Low cycles per second, large code sizes
• Transistors used for storing complex instructions	• Spends more transistors on memory registers
Examples of CISC processors: • VAX • PDP?11 • Motorola 68000 family • Intel x86 architecture based processors.	**Examples** of RISC processors • Apple iPods (custom ARM7TDMI SoC) • Apple iPhone (Samsung ARM1176JZF) • Nintendo Game Boy Advance (ARM7) • Sony Network Walkman (Sony in?house ARM based chip)

1.5 Flynn's Classification of Processors

1.5.1 Single Instruction Stream, Single Data Stream (SISD)

A computer with a single processor is called a Single Instruction Stream, Single Data Stream (SISD) Computer. It represents the organization of a single computer containing a control unit, a processor unit, and a memory unit. Instructions are executed sequentially and the system may or may not have internal parallel processing. Parallel processing may be achieved by means of a pipeline processing.

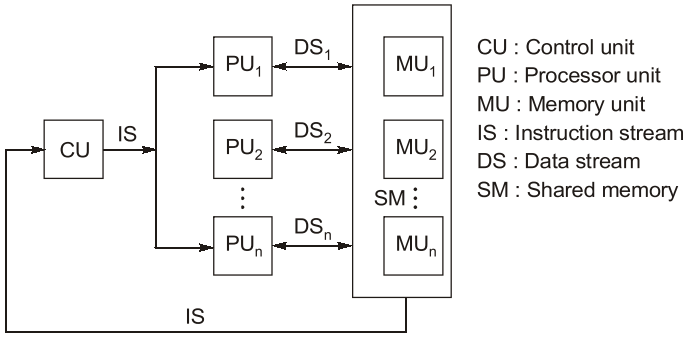
In such a computer a single stream of instructions and a single stream of data are accessed by the processing elements from the main memory, processed and the results are stored back in the main memory. SISD computer organization is shown in figure below.



1.5.2 Single Instruction Stream, Multiple Data Stream (SIMD)

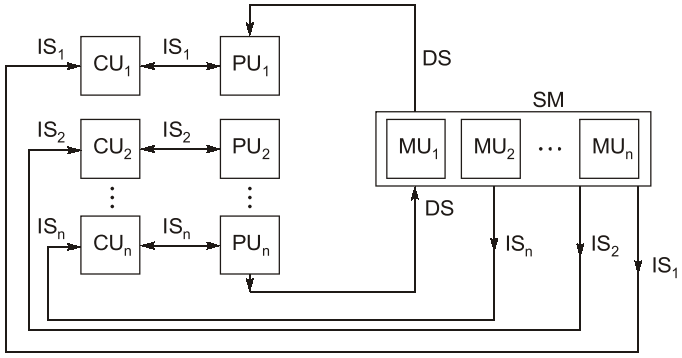
It represents an organization of computer which has multiple processors under the supervision of a common control unit. All processors receive the same instruction from the control unit but operate on different items of the data. SIMD computers are used to solve many problems in science which require identical operations to be applied to different data set synchronously. Examples are added a set of matrices simultaneously, such as $\sum_i \sum_k (a_{ik} + a_{ik})$.

Such computers are known as array processors. SIMD computer organization is shown in figure below.



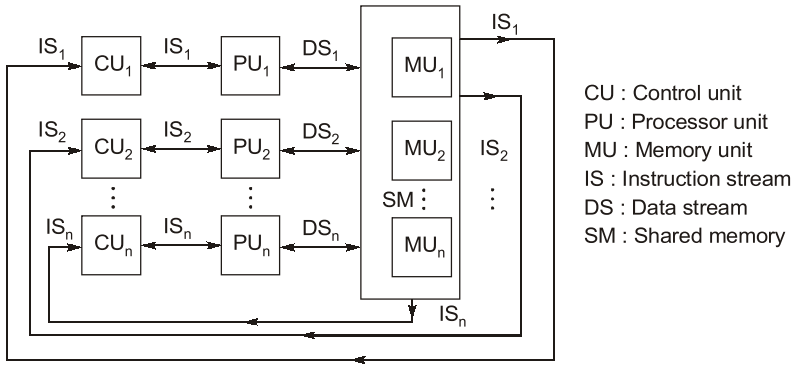
1.5.3 Multiple Instruction Stream, Single Data Stream (MISD)

It refers to the computer in which several instructions manipulate the same data stream concurrently. In the structure different processing element run different programs on the same data. This type of processor may be generalized using a 2-dimensional arrangement of processing element. Such a structure is known as systolic processor. MISD computer organization is shown in figure below.



1.5.4 Multiple Instruction Stream, Multiple Data Stream (MIMD)

MIMD computers are the general purpose parallel computers. Its organization refers to a computer system capable of processing several programs at a same time. MIMD systems include all multiprocessing systems. MIMD computer organization is shown in figure below.]



1.6 Control Unit

Control unit generates the signals for sequencing the operations in the datapath. It performs the task by repeatedly cycling through fetch-execute cycle steps:

- Read the instruction that's pointed to by the PC from memory and move it into the IR.
- Increment the PC.
- Decode the instruction in the IR.
- If the instruction has to read an operand from memory, calculate the operand's address (*effective address*) and read the operand from memory.
- Execute the current instruction from the IR.

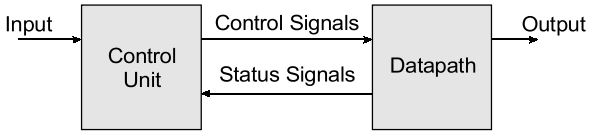
To execute an instruction, the control unit of the CPU must generate the required control signal in the proper sequence.

Functions of Control Unit

1. **Fetch and instruction sequencing:** Generates control signal to fetch instruction from memory and the sequence of operations involved in processing an instruction.
2. **Instruction interpretation and execution:**
   - Interpreting the operand addressing mode implied in the operation code and fetching the operands.
   - Sequencing the successive micro operations on the data path to execute the operation code specified in the instruction.

3. **Interrupt processing:** Process unmasked interrupts in the interrupt cycle as follows:
   - Suspend execution of current program
   - Save context
   - Set PC to start address of interrupt handler routine
   - Process interrupt
   - Restore context and continue interrupted program

Control Unit and Datapath

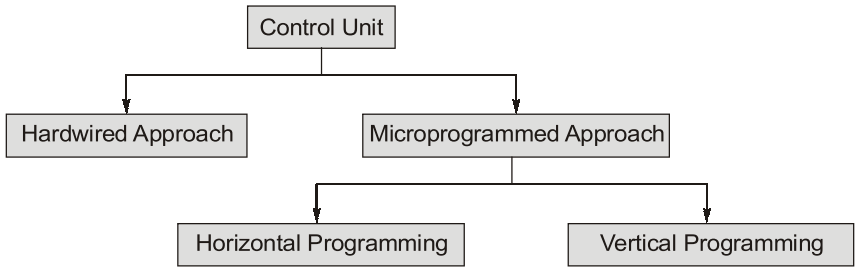


Control Unit: It generates the signals for sequencing the micro-operations in the datapath based on status and input signals.

Datapath: It implements the micro-operations under control of the control unit using its functional units (registers, ALU, MUXes, Buses, etc.)

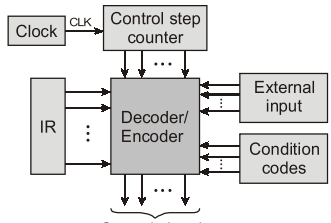
1.7 Control Unit Implementation

The main objective of control unit is to generate the control signal in proper sequence. Control unit is implemented in one of two ways either Hardwired control or Micro-programmed control.



1.7.1 Hardwire Control Unit

Hardwire Control unit is made up of sequential and combinational circuits (Hardware) to generate the control signals.



Control Unit Organization

Decoder/Encoder Block

It is a combinational circuit that generates the required control signals depending on the state of all its input.

(*i*) Step Decoder: The decoder part of decoder/encoder part provide a separate signal line for each control step, or time slot in the control sequence.

(*ii*) Instruction Decoder: The output of the instructor decoder consists of a separate line for each machine instruction loaded in the IR, one of the output line INS_1 to INS_m is set to 1 and all other lines are set to 0.

(*ii*) Encoder: It is required to generate many control signals by the control unit. These are basically coming out from the encoder circuit of the control signal generator.
The control signals are: PC_{in}, PC_{out}, Z_{in}, Z_{out}, MAR_{in}, ADD, END, etc.

The encoder sends a reset signal after the end of an instruction and a stop signal to the sequencer after the last sequence. The encoder also sends count start signal to let the clock increment the counter during processing of an instruction.

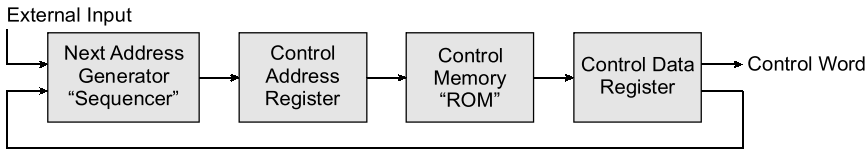
The advantage of hardwired control is that is very fast. The disadvantage is that the instruction set and the control logic are directly tied together by special circuits that are complex and difficult to design or modify.

The control signals are expressed as Sum-of-Product (SOP) expression and they are directly realized on the independent hardware.

1.7.2 Microprogrammed Control Unit

A control unit whose binary control variables are stored in memory is called a micro-programmed control unit. A control memory (Control storage) on the processor contains micro-programs that activate the necessary control signals whereas hardwired control unit generate control signals by sequential and combinational circuits.

- **Microinstruction:** The microinstruction specifies one or more micro-operations for the system. It contains a control word and a sequencing word.
- **Microprogram:** A sequence of microinstructions called a microprogram. Program stored in memory that generates all the required control signals to execute the instruction set correctly.



Control Memory (Control Storage): It is Memory unit in the micro-programmed control unit to store the micro-program. Each word in control memory contains within it a microinstruction.

Control Address Register: It specifies the address of the microinstruction in control memory.

Control Data Register: It holds the microinstruction read from memory.

The location of the next microinstruction may be the one next in sequence, or it may be locate somewhere else in the control memory. This reason it is necessary to use some bits of the present microinstruction to control the generation of the address of the next microinstruction.

The next address may also be a function of external input conditions. While the microoperations are being executed, the next address is computed in the next address generator circuit and then transferred into the control address register to read the next microinstruction.

Sequencing Word: Information needed to decide the next microinstruction address.

Next Address Generator (Sequencer or Microprogram Sequencer): It determines the microinstruction Address to be executed in the next clock cycle.

The address of the next microinstruction can be specified several ways, depending on the sequencer inputs as follows:

(*i*) Incrementing the control address register by one,
(*ii*) Loading into the control address register by an address from control memory,
(*iii*) Transferring an external address, or
(*iv*) Loading an initial address to start the control operations.

Determining the address of the next microinstruction depends on one of the following:

- In-line Sequencing
- Branch
- Conditional Branch
- Subroutine
- Loop
- Instruction op-code mapping

Let the main memory contains n blocks (which require $\log_2(n)$ bits of physical address) and cache contains m blocks. A given memory block can be mapped into one and only cache line (block). Here, n/m different blocks of memory can be mapped (at different times) to a cache block. Each cache block has a tag saying which block of memory is currently present in it, each cache block also contain a valid bit to ensure whether a memory block is in the cache block currently.

- Number of bits in the tag = log (n/m)
- Number of sets (or blocks) in the Cache = m
- Number of bits to identify the correct Block = log (m)
- Number of Sets in cache = Number of Blocks in cache
- Each set contain only one block, so in direct cache mapping set is also called as block.
- INDEX is used to select the memory block.
- TAG is used to select the cache block from main memory set
- Select location within block using block offset.
- TAG + INDEX = Block Address

***Example* - 1.1** A 32 bits byte address Direct-mapped cache defined as:

Cache size = 2^n block, n bits used for index

Block size = 2^m block, m bits for word between block, 2 used for byte part of address

Size of tag field : 32 – (m + n + 2)

One valid bit field is used in cache.

Find the direct mapped cache size (in bits).

Solution:

Total number of bits in direct-mapped cache = 2^n x (block size + tag size + valid field size)

Block size = 2^m words

1 bit valid field is needed.

$$\text{Cache size} = 2^n \times (2^m \times 32 + 32 - n - m - 2) + 1) \text{ bits}$$
$$= 2^n \times (2^m \times 32 + 31 - n - m) \text{ bits}$$

***Example* - 1.2** How many total bits are required for a direct-mapped cache with 16 kB of data, 1 bit field for valid and 4-word blocks, assuming a 32-bit address?

Solution:

16 kB = 2^{12} words of data, 4 words block size (= 2^2).

So, there are 1024 blocks (= 2^{10})

$$\text{Tag} = 32 - 10 - 2 - 2 \text{ bits}$$
$$\text{Cache Entry size} = 128 \text{ bits of data + tag bits + valid bit.}$$
$$\text{Cache size} = 2^{10} \text{ x (4 x 32 + (32 – 10 – 2 – 2) + 1}$$
$$= 2^{10} \text{ x 147 = 147 K bits}$$

1.9.4 Fully Associative Cache

- It is also called as m-way set associative cache, where m is number of blocks and all blocks fit into one set.
- Instead of using a cache index, compare the tags of all cache entries in parallel
- Because no bit field in the address specifies a line number the cache size is not determined by the address size.

Solution:

	1	2	3	2	1	5	2	1	6	2	5	6	3	1	3	6	1	2	4	3
	1	1	1	1	3	2	1	5	2	1	6	2	5	6	6	1	3	6	1	2
		2	2	3	2	1	5	2	1	6	2	5	6	3	1	3	6	1	2	4
			3	2	1	5	2	1	6	2	5	6	3	1	3	6	1	2	4	3
	x	x	x			x			x		x		x	x				x	x	x

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Summary

- **Computer:** A device that accepts input, processes data, stores data, and produces output, all according to a series of stored instructions.
- **Hardware:** Includes the electronic and mechanical devices that process the data; refers to the computer as well as peripheral devices.
- **Software:** A computer program that tells the computer how to perform particular tasks.
- **Computer organization:** Interconnection of hardware to form the computer system
- **Computer architecture:** the structure and behaviour of the computer perceived by the user.
- **Input:** The data or raw information entered into a computer.
- **Data:** Refers to the symbols that represent facts, objects, or ideas.
- **Information:** The results of the computer storing data as bits and bytes; the words, numbers, sounds, and graphics.
- **Output:** Consists of the processing results produced by a computer.
- **Main Memory:** Area of the computer that temporarily holds data waiting to be processed, stored, or output. *Example:* Cache and Main memory
- **Secondary Storage:** Area of the computer that holds data on a permanent basis when it is not immediately needed for processing. Example: Disk, Floppy, etc.

Student's Assignments

Q.1 What does CISC and RISC means?
(a) common instruction set controller and rare instruction set controller
(b) complex instruction set controller and reduced instruction set controller
(c) compiled instruction set source code and recompiled instruction source code
(d) none of the above

Q.2 A 32-bit address bus allows access to a memory of capacity
(a) 64 Mb (b) 16 Mb
(c) 1 Gb (d) 4 Gb

Q.3 The system bus is made up of
(a) data bus
(b) data bus and address bus
(c) data bus and control bus
(d) data bus, control bus and address bus

Q.4 Which of the following is not involved in a memory write operation?
(a) MAR (b) PC
(c) MDR (d) data bus

Q.5 The read/write line
(a) belongs to the data bus
(b) belongs to the control bus
(c) belongs to the address bus
(d) CPU bus

Q.6 _____ is a piece of hardware that executes a set of machine-language instructions.
(a) controller (b) bus
(c) processor (d) motherboard

Q.7 Given below are some statements associated with the registers of a CPU. Identify the false statement.
(a) The program counter holds the memory address of the instruction in execution.
(b) Only opcode is transferred to the control unit.
(c) An instruction in the instruction register consists of the opcode and the operand.
(d) The value of the program counter is incremented by 1 once its value has been read to the memory address register.

Q.8 In Flynn's classification of computers, the vector and array classes of machines belong to
(a) Single instruction/single data category
(b) Single instruction/multiple data category
(c) Multiple instruction/single data category
(d) Multiple instruction/multiple data category

Q.9 The following are four statements regarding what a CPU with only a set of 32 bit registers can perform.
1. Hold and operate on 32 bit integers
2. Hold and operate on 16 bit integers
3. Hold and operate on 64 bit floating point arithmetic
4. Hold and operate on 16 bit UNICODE characters

Which of the following is true about such a CPU?
(a) all are true (b) 1,2 and 3 only
(c) 1,2 and 4 only (d) 1,3 and 4 only

Q.10 The following are four statements about Reduced Instruction Set Computer (RISC) architectures.
1. The typical RISC machine instruction set is small, and is usually a subset of a CISC instruction set.
2. No arithmetic or logical instruction can refer to the memory directly.
3. A comparatively large number of user registers are available.
4. Instructions can be easily decoded through hard-wired control units.

Which of the above statements is true?
(a) 1 and 3 only (b) 1,3 and 4 only
(c) 1, 2 and 3 only (d) All of these

Q.11 The word length of a CPU is defined as
(a) the maximum addressable memory size
(b) the width of a CPU register (integer or float point)
(c) the width of the address bus
(d) the number of general purpose CPU registers

Q.12 Which of the following statements is false about CISC architectures?
(a) CISC machine instructions may include complex addressing modes, which require many clock cycles to carry out.
(b) CISC control units are typically micro-programmed, allowing the instruction set to be more flexible.
(c) In the CISC instruction set, all arithmetic/logic instructions must be register based.
(d) CISC architectures may perform better in network centric applications than RISC.

Q.13 Which one is required while establishing the communication link between CPU and peripherals?
(a) synchronization mechanism
(b) conversion of signal values
(c) operating modes
(d) all of the above

Q.14 What will be average cost per bit for a system with main memory of 1024 cost, 100 units and secondary memory of 4096 cost, 10 units.
(a) 35.7 (b) 28.0
(c) 82.0 (d) insufficient data

Q.15 Consider a Disk I/O transfer, in which 1500 bytes are to be transferred, but number of bytes on a track is 1000, and rotation speed of disk is 1500 rps but the average time required to move the disk arm to the required track is 15 ms, then what will be total access time?
(a) 16.33 ms (b) 15.33 ms
(c) 16.33 μs (d) 15.33 μs

Q.16 A disc drive has a rotational speed of 3600 rpm, an average seek time of 10 ms, 64 sectors per track and 512 bytes of data per sector. What is the average time to access the entire data of a 16 kbytes file stored sequentially on the disk?
(a) 18.85 ms (b) 10 ms
(c) 27.15 ms (d) 9 ms

Q.17 The seek time of a disk is 30 msec. It rotates at the rate of 30 rotations per second. Each track has a capacity of 300 words. The access time is
(a) 47 msec (b) 50 msec
(c) 60 msec (d) 62 msec

Q.18 A disc drive has a average seek time of 10 ms, 32 sectors on each track and 512 bytes per sector. If the average time to read 8 kbytes of continuously stored data is 20 ms, what is the rotational speed of the disc drive?
(a) 3600 rpm (b) 6000 rpm
(c) 3000 rpm (d) 2400 rpm

Q.19 A disc rotates at a speed of 7200 rpm. It has 4000 cylinders, 16 surfaces and 256 sectors per track. What is the average latency time of the disk?
(a) 8.33 ms (b) 4.166 ms
(c) 41.66 ms (d) 8.33 ms

Q.20 A magnetic drum of 8 inch diameter has 100 tracks and storage density of 200 bits/inch. What is its storage capacity?
(a) 8402 bits (b) 202400 bits
(c) 502400 bits (d) 1004800 bits

Q.21 Match **List-I** (Type of Memory) with **List-II** (Access time in μsec/nsec) and select the correct answer using the code given below the lists:

List-I	List-II
A. DRAM	1. 1
B. SRAM	2. 10
C. Hard Disk	3. 100000
D. Magnetic Tape	4. 10000000

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	1	2	4	3
(c)	2	1	3	4
(d)	2	1	4	3

Q.22 The difference between memory and storage 1's that the memory is _____ and the storage is _____.
(a) Temporary, Permanent
(b) Permanent, Temporary
(c) Slow, Fast
(d) None of these

Q.23 Which of the following holds, the ROM, CPU, RAM and Expansion cards?
(a) Hard disk (b) Floppy disk
(c) Mother board (d) None of these

Q.24 Information retrieval is faster from
(a) Floppy disk (b) Magnetic tape
(c) Hard disk (d) Cassette tape

Q.25 Winchester disk is a
(a) Disk stack (b) Removable disk
(c) Flexible disk (d) None of these

Q.26 Magnetic tapes are good storage media for
(a) backup and low volume data
(b) backup and high voltage data
(c) storing original but low volume data
(d) storing original but high volume data

Q.27 What is the control unit's function in the CPU?
(a) to decode program instructions
(b) to transfer data to primary storage
(c) to perform logical operations
(d) to store program instructions

Q.28 Which of the following affects processing power?
(a) data bus capacity
(b) addressing scheme
(c) clock speed
(d) all of the above

Q.29 A _____ is required to translate such microprogram into executable programs that can be stored in the control memory in microprogramming.
(a) microassembler
(b) microcompiler
(c) microprogrammed CPU
(d) microprogrammed counter

Q.30 Microinstruction length is determined by _____.
1. The maximum number of simultaneous micro operations that must be specified.
2. The way in which the control information is represented or encoded.
3. The way in which the next microinstruction address is specified.

(a) 1 and 2 (b) 2 and 3
(c) 1 and 3 (d) all of the above

Q.31 Horizontal microinstruction have which of the following attributes?

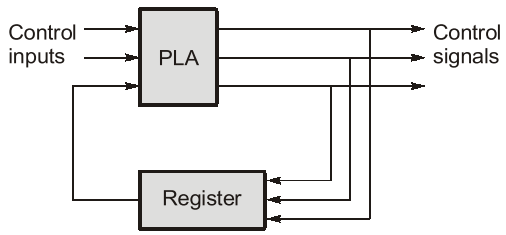
1. Short formats
2. Limited ability to express parallel micro operations
3. Considerable encoding of the control information

(a) 1 and 2 (b) 2 and 3
(c) 1, 2 and 3 (d) None of these

Q.32 Asynchronous data transfer between two independent units requires that control signals be transmitted between the communicating units to indicate the time at which data is being transmitted, way of achieving this _____.

(a) Is by means of a strobe pulse from one of the unit
(b) Is by means of handshaking
(c) Both (a) and (b)
(d) None of these

Q.33 Consider the following figure



The above circuit represents _____.

1. Hard-wired control unit
2. Micro programmed control unit

(a) Only 1 (b) Only 2
(c) Both 1 and 2 (d) Either 1 or 2

Q.34 Pipelining improves CPU performance due to

(a) reduced memory access time
(b) increased clock speed
(c) the introduction of parallelism
(d) additional functional units

Q.35 Which of the following statements is false with regard to instruction pipelining?

(a) The basic goal of instruction pipelining is to achieve a CPI of 1.
(b) Instruction set architectures having simple registry/register addressing modes can be easily pipelined than those having complex addressing modes.
(c) By the use of hardware special features and compiler design techniques, pipeline hazards can be removed.
(d) The basic goal of instruction pipelining is to achieve a CPI of more than 1.

Q.36 **Assertion (A):** Reduced Instruction Set Computers (RISC) use pipelined control unit.
Reason (R): Pipelining reduces memory requirements of programs.

(a) Both A and R are true and R is the correct explanation of A
(b) Both A and R are true but R is NOT the correct explanation of A
(c) A is true but R is false
(d) A is false but R is true

Q.37 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Pipelined ALU
B. Simpler compiler
C. Separate data and instruction caches
D. Lesser cycles per instruction

List-II

1. RISC
2. CISC
3. Mixed
4. Mixed RISC-CISC

Codes:

	A	B	C	D
(a)	3	2	3	1
(b)	1	2	3	3
(c)	3	3	2	1
(d)	3	3	3	1

Answer Key :

1. (d)	**2.** (d)	**3.** (d)	**4.** (b)	**5.** (b)
6. (c)	**7.** (a)	**8.** (b)	**9.** (c)	**10.** (d)
11. (b)	**12.** (c)	**13.** (d)	**14.** (b)	**15.** (a)
16. (c)	**17.** (b)	**18.** (d)	**19.** (b)	**20.** (c)
21. (c)	**22.** (a)	**23.** (c)	**24.** (c)	**25.** (a)
26. (b)	**27.** (a)	**28.** (d)	**29.** (a)	**30.** (d)
31. (d)	**32.** (c)	**33.** (c)	**34.** (c)	**35.** (d)
36. (a)	**37.** (a)			