Electronics Engineering

Advanced Electronics

Comprehensive Theory

with Solved Examples and Practice Questions

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Advanced Electronics

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CHAPTER 1

Integrated Circuits Fabrication Technology

Introduction

In an integrated circuit, all the circuit components, that is diodes, transistors, resistors, capacitors as well as the interconnections among them are realized on a single semiconductor chip. A large number of process steps are involved in the fabrication of semiconductor devices for integrated circuits. To begin with, the semiconductor material must be in the form of single crystals with defect-free surfaces. Controlled amount of impurities must then be introduced in the substrate to achieve proper doping. This may involve protecting particular regions of the substrate (masking), so that the doping occurs only in selected regions. This is followed by metallization to realize electrical contacts, scribing the devices into individual dies, attaching leads and finally encapsulation (packaging). This chapter discusses the various unit processes used in IC fabrication.

1.1 Crystal Growth

As already pointed out, for the fabrication of semiconductor devices, the substrate must be in single crystal form. Silicon, the most commonly used semiconductor, is abundantly available on the earth's surface in the form of sand, which is almost pure silica (SiO_2). After chemical purification and reduction of silica, very pure (99.9999%) polycrystalline silicon is obtained, which is used as the starting material for single crystal growth. Single crystal silicon for integrated circuits is mostly grown by two methods, namely the Czochralski (CZ) and the Float Zone (FZ) techniques.

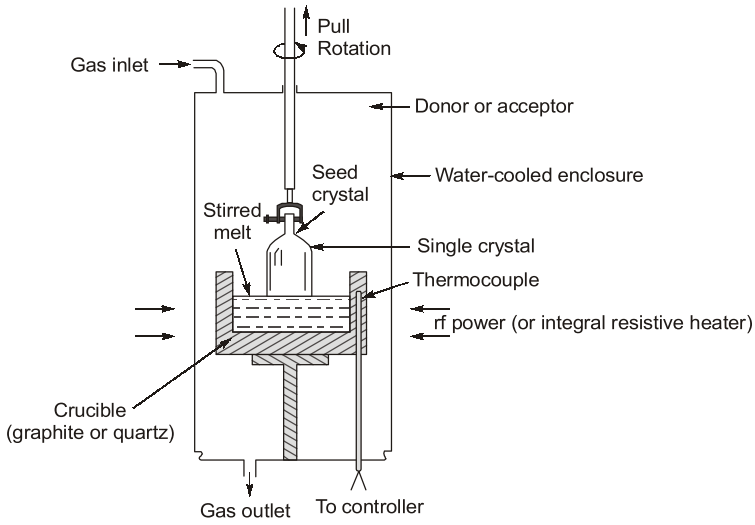


Figure-1.1 : *Czochralski crystal growth system*

In the CZ technique, the polycrystalline material is kept in a quartz crucible held in a graphite susceptor and is heated by rf or resistive heating. Once the polycrystalline charge melts, a seed of single crystal suspended above the melt, is slowly lowered and brought into contact with the melt. The crystal is now slowly pulled up while rotating the crucible. A larger crystal starts to grow as the melt in contact with the seed solidifies. The whole system is kept inside a chamber that is flushed with an inert gas such as argon. Figure 1.1 shows the basic arrangement for this growth technique. Materials with desired doping concentrations are grown by introducing appropriate impurities into the melt.

The crystals grown by CZ technique have appreciable oxygen content (10^{17}-10^{18} cm) from the reaction of the melt with quartz crucible. On the other hand, no crucibles are used in FZ technique resulting in higher purity silicon. In this method, a rod of high-purity polycrystalline silicon is held vertically in a chamber with an inert ambience. A seed of single crystal is clamped at the lower end of this rod. An rf heater coil is brought close to the seed-end of the rod and a small portion of the rod is melted. As the heating coil is moved slowly upwards, the molten portion in contact with the seed crystallizes, assuming the crystal structure of the seed. Just above this, a new molten zone is formed and the process continues. Oxygen levels in FZ-grown crystals are only of the order of 10^{15} per cm^3.

The semiconductor crystals grown by either of the two techniques just described are next cut into thin discs called wafers. The thickness of these wafers is approximately 500 μm to 1 mm, while the diameter is 15-25 cm for standard silicon samples currently in use. These wafers, which are then chemo-mechanically polished to obtain a mirror-like finish on one side, are now ready for fabrication. Wafers used in device fabrication usually have a {111} or a {100} crystal orientation.

1.2 Doping and Impurities

In order to fabricate semiconductor devices, a controlled amount of impurities has to be introduced (doped) selectively into single crystal wafers. There are three basic methods used for controlled doping of a semiconductor, namely epitaxy, diffusion, and ion-implantation. These methods are dealt with in the subsequent sections.

1.2.1 Epitaxy

The term epitaxy literally means "arranged upon". In this process, a thin layer of single crystal semiconductor (typically a few nanometers to a few microns) is grown on an already existing crystalline substrate such that the film has the same lattice structure as the substrate. Epitaxy can be further classified into Vapour Phase Epitaxy (VPE), Liquid Phase Epitaxy (LPE), and Molecular Beam Epitaxy (MBE).

Epitaxial growth of silicon is almost exclusively carried out by VPE. In this method, silicon is deposited by chemical vapour deposition (CVD) from source materials such as $SiCl_4$ $SiHCl_3$, and SiH_2CL_2. The silicon wafer (on which epitaxial growth occurs) is placed on a graphite susceptor kept in a quartz chamber. Hydrogen gas is passed through liquid $SiCl_4$ and the mixture of $SiCl_4$ and H_2 is passed through this quartz tube. The system is rf-heated to a temperature above 1100°C. The schematic diagram of a VPE reactor is shown in Fig. 1.2. The basic reaction that occurs on the silicon surface in the process is

$$SiCl_4 + 2H_2 \Leftrightarrow Si + 4HCl$$

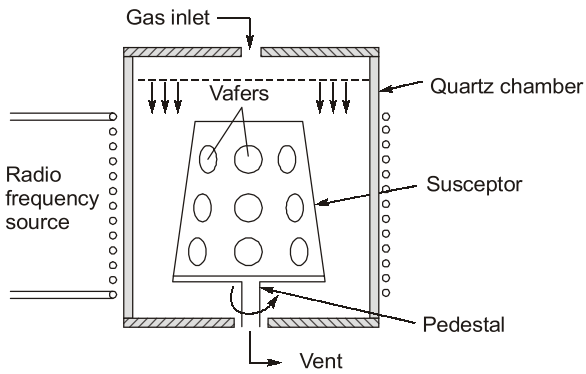


Figure-1.2: *Schematic diagram of a VPE reactor with barrel-shaped susceptor*

The reaction is surface-catalyzed and silicon is deposited on the wafer surface. However, the deposition temperature is very high. Also, as the reaction is reversible and can proceed in both directions, etching, instead of deposition, may sometimes occur. Alternatively, SiH_4 may be used as a source material. Pyrolytic decomposition of SiH_4 at 1000-1100°C results in deposition of epitaxial silicon by the following reaction:

$$SiH4 \rightarrow Si + 2H_2T$$

In order to grow epitaxial layer of silicon with desired doping, gases containing dopants such as PH_3, AsH_3, or B_2H_6 are introduced into the system.

Molecular beam epitaxy (MBE) uses vacuum evaporation technique to grow epitaxial layers with very high degree of control. The substrate is held in ultra-high vacuum and epitaxial layers are deposited on the heated substrate from molecular beams impinging upon its surface. These beams are thermally generated in effusion cells (Knudsen cells) containing the constituent elements (such as Ga, As, and so on) of the desired layer. Each cell has a shutter to control the composition and/or doping of the film. The temperature of the cell is also accurately controlled to maintain the required intensity of the beams. Because of the ultra-high vacuum and precise control requirements, MBE systems are very expensive. However, the quality of the films is very good with precise control of doping. A schematic diagram of an MBE system is shown in Fig. 1.3.

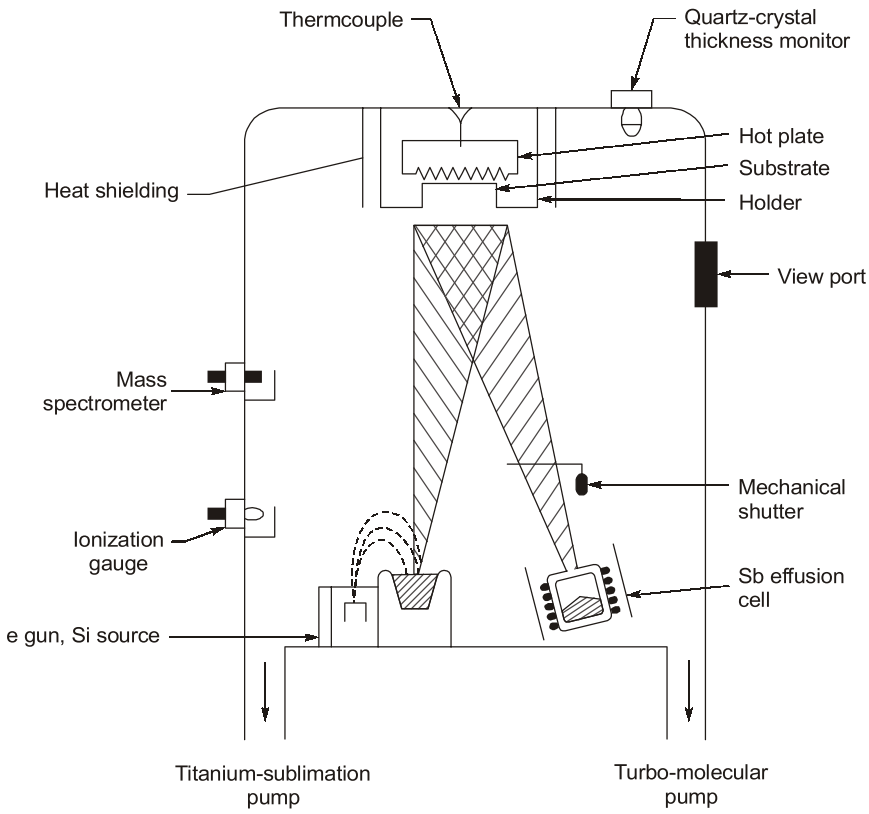


Figure-1.3 : *Schematic diagram of MBE*

1.2.2 Diffusion

Although, it is possible to grow a layer with controlled doping by epitaxy, it is not possible to control the doping of particular regions of the semiconductor surface. In other words, epitaxial growth takes place on the entire surface, that is, it is nonselective. In order to achieve selective doping, the technique most commonly used in silicon processing is called diffusion. The basic principle underlying this process is that the dopant atoms migrate from a region of high concentration to a region of low concentration. Some portions of the semiconductor

are covered by a masking material, while the rest is left unprotected. Now if the semiconductor is held in an ambience of high dopant concentration and the temperature is raised, dopant atoms migrate into the unprotected regions of the semiconductor while many semiconductor atoms move out of their regular lattice sites. The dopant atoms may either move into these vacant sites **(substitutional impurities)** or occupy the empty space in between the lattice atoms **(interstitial impurities).** On cooling the sample, interstitial atoms may occupy substitutional positions and thus, become electronically active. Most common dopants in silicon, for example, phosphorus and boron, occupy substitutional sites, that is, they replace silicon atoms in the lattice. In practice, usually a two-step process is adopted to dope silicon.

Predeposition: In the first step (also called predeposition), the sample is heated in the presence of a very high concentration of the dopant. Under this condition, the diffusion profile is given by

$$N(x, t) = N_0 \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) + N_B \qquad ...(1.1)$$

where, N_B = original doping concentration of the sample,

N_0 = solid solubility of the dopant in the semiconductor at the process temperature,

D = diffusion coefficient of the dopant in the semiconductor at the process temperature,

and t = diffusion time

x = distance from the sample surface.

From the above equation, we can see that after predeposition, the surface concentration $N(0, t)$ will always be No (since usually $N_0 >> N_B$), which is a constant for a given temperature. The doping profiles for different durations of predeposition are shown in Fig. 1.4 (a). The total number of impurity atoms per unit area of the semiconductor surface introduced in this step is

$$Q(t) = \int_0^\infty [N(x,t)]dx = 2N_0\sqrt{\frac{Dt}{\pi}} \qquad ...(1.2)$$

Drive-in: In the next step (called drive-in), the dopant source is shut off and the sample is heated further. The doped layer already present on the sample surface now acts as the dopant source and the doping profile is given by

$$N(x, t) = \frac{Q}{\sqrt{\pi Dt}} \exp\left(-\frac{x^2}{4Dt}\right) + N_B \qquad ...(1.3)$$

Equation (1.3) represents a Gaussian plot. An examination of Eq. (1.3) reveals that for longer durations of drive-in, the surface impurity concentration decreases while the impurities move deeper into the substrate increasing the junction depth. The doping profiles for different drive-in durations are shown in Fig. 1.4 (b).

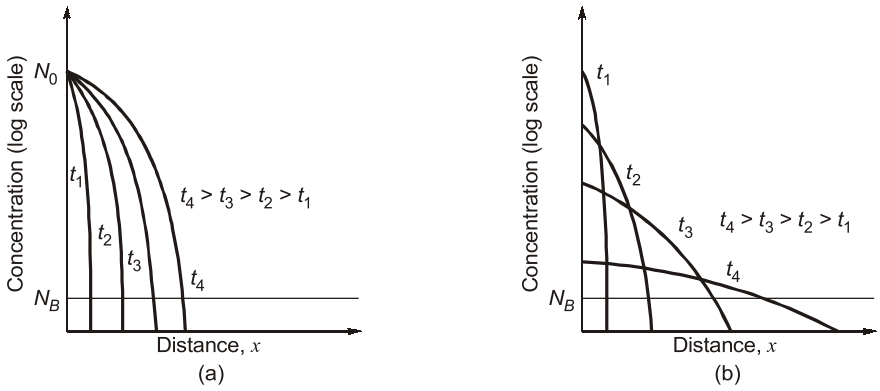


Figure-1.4: *Doping profiles with different durations (a) predeposition and (b) drive-in*

Example - 1.1 Phosphorus is diffused into a uniformly doped p-type silicon with original doping concentration of the sample being 10 per cm at 1150°C. Given that the solid-solubility of phosphorus in silicon at 1150°C is $10^{20}/cm^3$ and the diffusion coefficient at this temperature is $10^{-12}\ cm^2\ s^{-1}$, (a) calculate the total number of phosphorus atoms per unit area of the silicon surface after a predeposition time of 1 hour, (b) If after this, drive-in is carried out for 2 hours at the same temperature, what will be the final junction depth and the surface concentration?

Solution:

(a) From Eq. (1.2), we obtain the total amount of phosphorus introduced in silicon per unit area after predeposition as

$$Q = 2\times10^{20}\sqrt{\frac{10^{-12}\times3600}{\pi}} = 6.77\times10^{15}\ \text{per cm}^2$$

(b) Now after drive-in, the surface concentration is given by setting $x = 0$ in Eq. (1.3). So, if the drive-in is carried out for 2 hours at the same temperature, we have

$$N = \frac{6.77\times10^{15}}{\sqrt{\pi\times10^{-12}\times7200}} - 10^{16} = 4.5\times10^{19}\ \text{per cm}^3$$

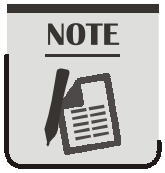
The negative sign for N_B implies that the original substrate dopant and the diffused impurity are of opposite types.

In order to obtain the junction depth, we note that at the junction the phosphorus concentration becomes equal to the original background doping concentration of the sample, that is, $N(x_j, t) = 0$. Substituting this in Eq. (1.3), we get

$$\exp\left(\frac{x_j^2}{4\times10^{-12}\times7200}\right) = \frac{4.5\times10^{19}}{10^{16}}$$

This gives the junction depth as $x_j = 4.92\ \mu m$.

The common *n*-type dopants in silicon are the group V elements such as phosphorus, arsenic, and antimony while the group III element boron is almost exclusively used for p-type doping. Usually, diffusion in silicon is carried out in an open-tube furnace. A gas mixture carrying the dopant is made to flow over the sample kept in a carefully controlled atmosphere. The dopant source may be a solid, liquid, or gas. $POCl_3$ is the preferred liquid source used for doping phosphorus, though gaseous dopants such as PH_3 may also be used. BN (solid source) or BBr_3 (liquid) are the commonly used dopant sources for boron diffusion. Whatever be the actual dopant source, in all the cases, it is made to react with oxygen at high temperature to form an oxide (D_xO_y, where *D* is the dopant element, say, *P* or *B*). This oxide then reacts with the silicon surface forming SiO_2 and releases the dopant into the semiconductor.



Although gallium is a group III element, why is it not commonly used as a p-type dopant in silicon? Theoretically, group III elements such as Al or Ga, which have sufficiently low ionization energies can be used as p-type dopants in silicon. However, the diffusivity of these materials in SiO_2, which is the most commonly used masking material, is very high. During diffusion, Ga therefore has a tendency to diffuse in the regions protected by SiO_2. As the diffusivity of boron in SiO_2 is very small, such problems are not encountered in boron diffusion. Boron is thus exclusively used as the p-type dopant in silicon technology.

1.2.3 Ion Implantation

Ion implantation is an alternative technique used for selective doping of semiconductors. The doping profile is more precisely controlled by this technique. Also, it is a low temperature process. Another advantage of ion implantation is that it allows the doping profile to be tailored with a greater degree of flexibility. For example, from Eqs. (1.1) and (1.3) as well as Figs. 1.4 (a) and (b), we see that in a diffusion process, the peak impurity concentration always occurs at the surface. However, by ion implantation, it is even possible to attain the peak concentration below the surface. These advantages make ion implantation a very important process step in the present day MOS as well as Bipolar Transistor technologies.

In ion implantation, a beam of high-energy dopant ions is made to impinge on the semiconductor surface. When these ions enter the semiconductor, they lose their kinetic energy through collisions with the electrons as well as the nuclei of the lattice atoms. Finally, an impurity atom comes to rest when its kinetic energy falls to zero. The distance perpendicular to the semiconductor surface covered by the impurity atom before coming to rest is called its *projected range* (R_p). Obviously, the projected range for a particular impurity species depends upon the energy *(E)* of the ion beam. In an amorphous material the doping after implantation is given by

$$N(x) = \frac{Q_0}{\Delta R_p \sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{x - R_p}{\Delta R_p}\right)^2\right] \quad ...(1.4)$$

where, AR_p = standard deviation of the projected range and

Q_0 = total implantation dose (number of impurity ions introduced per unit area).

The implantation dose depends on the ion beam current density J and the implantation time t and is expressed as

$$Q_0 = \frac{Jt}{q} \quad ...(1.5)$$

Since the implantation dose depends only on the current and time, it can be very precisely controlled. From Eq. (1.4), it is evident that the peak impurity concentration occurs at $x = R_p$, that is, where the maximum number of dopant ions come to rest. By varying the energy of the ion beam, it is possible to obtain implantation very close to the surface or deep inside as the requirements may be. Figure 1.5 shows the actual implantation profiles for boron in silicon for different ion-beam energies.

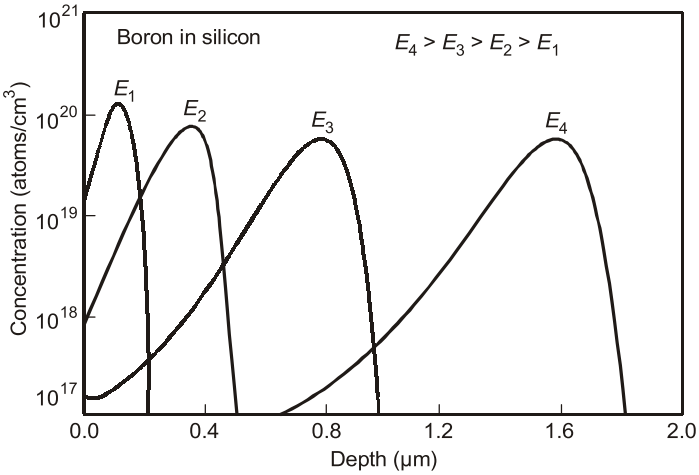


Figure-1.5: *Actual implantation profile for boron in silicon for different values of ion-beam energy*

For a crystalline target, Eq. (1.4) is not valid. Due to the regularity of the crystal structure, the impurity ions may find an open corridor in between the lattice atoms when the ion beam is projected along a major crystallographic axis and can thus penetrate much deeper as shown in Figure 1.6. This is called channelling. Channelling can be particularly severe for low dose of implantation as shown in the figure. However, by tilting the substrate with respect to the ion beam direction, channelling can be reduced to a great extent. An alternative technique to reduce channelling is pre-amorphization in which the substrate surface is amorphized by bombarding with self-ions (that is, silicon surface bombarded with Si^+) before the actual implantation of the dopants. Sometimes, the implantation is also carried out through a thin (amorphous) oxide layer grown or deposited on the semiconductor surface to reduce channelling.

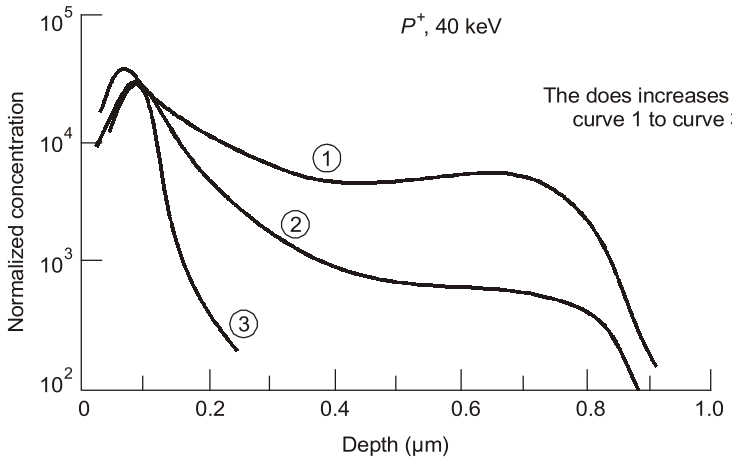


Figure-1.6: *Channeling of phosphorus in silicon at different implantation doses*

Example **- 1.2** Phosphorus is implanted in a p-type silicon sample with a uniform doping concentration of 10^{16} atoms per cm^3. If the beam current density is 2 μA per cm^2 and the implantation is carried out for ten minutes, calculate the implantation dose. Also find the peak impurity concentration. Assume R_p = 1.1 μm and ΔR_p = 0.3 μm.

Solution:

From Eq. (1.5), we obtain the value of the implantation dose as

$$Q_0 = \frac{2\times10^{-6}\times10\times60}{1.6\times10^{-19}} = 7.5\times10^{15}\ \text{cm}^{-2}$$

The peak impurity concentration occurs at x - $R.,.$ Substituting this value of x in Eq. (1.4), we get the peak concentration as

$$N_p = \frac{7.5\times10^{15}}{0.3\times10^{-4}\times\sqrt{2\pi}} = 9.97\times10^{19}\ \text{cm}^{-3}$$

Even though ion-implantation offers a lot of advantages over diffusion, the process of implantation creates a lot of damages in the implanted region. These defects have to be thermally annealed in order to make the doped region electronically active. Annealing can be carried out in a conventional furnace at a temperature range of 800-1000°C for 20-30 minutes. However, this may alter the doping profile considerably by driving the dopants in. Rapid thermal annealing (RTA) is an alternative technique in which the sample temperature is raised to a high value quickly, held constant for a brief period, and then cooled down fast. The entire annealing cycle may take a few seconds to a few minutes and the doping profile remains essentially unaltered. RTA is therefore preferred as an annealing technique in present day VLSI technology over conventional furnace annealing.

1.3 Growth and Deposition of Dielectric Films

In semiconductor processing, dielectric films essentially serve three purposes. They can be (i) a part of the active device (for example, gate oxide of a MOS transistor), (ii) used as masks to protect against diffusion (or ion-implantation), and (iii) used as a protecting layer (also known as passivation) at the end of device fabrication so as to protect the device from harsh ambience and ensure reliable operation. The most commonly used dielectric materials in semiconductor technology are SiO_2 and Si_3N_4. These films can either be grown on the semiconductor or deposited by using various techniques.

1.3.1 Thermal Oxidation of Silicon

Thermal oxidation is the most widely used technique to grow SiO_2 on silicon. This is usually carried out in an open-tube quartz furnace at a temperature range of 900-1200°C in an atmosphere of dry oxygen *(dry oxidation)* or water vapour *(wet oxidation).* For dry oxidation, oxygen is passed through the tube where it reacts with silicon to form SiO_2 by means of the following reaction

$$Si + 0_2 \rightarrow SiO_2$$

In case of wet oxidation, high purity de-ionized water, kept in a quartz bubbler at the inlet of the furnace, is heated to a temperature close to its boiling point. High purity oxygen or nitrogen is passed through it so that the gas flowing into the furnace is saturated with water vapour. Water then acts as the oxidizing agent and the oxidation reaction is given by

$$Si + 2H_20 \rightarrow SiO_2 + 2H_2\uparrow$$

The oxide thickness grown on silicon by the process of dry or wet oxidation is dependent on the oxidation time and temperature. This thickness can be expressed by a linear-parabolic relation represented as

$$d^2 + Ad = B\,(t + \tau) \qquad ...(1.6)$$

where, d = oxide thickness,

A and B = coefficients that depend on oxidation temperature and ambient conditions,

t = oxidation time, and

τ = a parameter for fitting the initial-value of oxide thickness.

For short duration of oxidation, $d << A$ and Eq. (1.6) can be approximated as

$$d = \frac{B}{A}(t + \tau) \qquad ...(1.7)$$

which signifies that when the oxidation is carried out for a short time, the oxide thickness grows linearly with time. The oxidation rate in this regime is limited by the surface reaction rate and is characterized by the linear rate constant (B/A).

The solution of Eq. (1.6) shows that for longer oxidation times, such that $(t + \tau) >> (A^2/4B)$, the oxide thickness can be expressed as

$$d = \sqrt{Bt} \qquad ...(1.8)$$

In this regime, the oxidation rate is primarily governed by the diffusion of the oxidizing agent through the already existing oxide layer and is characterized by the parabolic rate constant (B). The oxidation rate is much faster for wet oxidation than for dry oxidation. The crystal orientation also plays a role in the oxide growth process with {111} samples having thicker oxide films than {100} samples when oxidation is carried out under identical conditions.

Student's Assignments 1

Q.1 The advantage of IC over discrete component-based circuits is
(a) low power (b) small size
(c) low cost (d) all of these

Q.2 In the fabrication of a buried layer n-p-n transistor, the processes involved are
1. Diffusion 2. Oxidation
3. Epitaxy 4. Lithography
The correct sequence in which these processes are to be carried out, is
(a) 2, 4, 3, 1 (b) 4, 2, 1, 3
(c) 2, 4, 1, 3 (d) 4, 2, 3, 1

Q.3 A diffused resistor in an IC
(a) is fabricated before transistor diffusion
(b) is fabricated after transistor diffusion
(c) can be fabricated with precision for any resistance value
(d) is formed along with fabrication of transistors

Q.4 In integrated circuits, the design of electronic circuits is based on the approach of use of
(a) maximum number of resistors in the circuit
(b) large sized capacitor
(c) minimum chip area irrespective of the type of components in the design
(d) use of only bipolar transistors

Q.5 Silicon dioxide layer is used in IC chips for
(a) providing mechanical strength to the chip
(b) diffusing elements
(c) providing contacts
(d) providing mask against diffusion

Q.6 Which of the following is not the function of oxide layer during IC fabrication
(a) to increase the melting point of silicon.
(b) to mask against diffusion or ion implant.
(c) to insulate the surface electrically.
(d) to produce a chemically stable surface.

Q.7 Solid solubility of phosphorus in silicon
(a) remains constant at all temperature
(b) continuously increases with increase of temperature
(c) continuously decreases with increase of temperature
(d) first increases with temperature, reaches a maximum and then decreases with further increase in temperature

Q.8 The common p-type dopant in silicon is/are
(a) Boron
(b) Boron and Gallium
(c) Gallium
(d) Boron, Gallium and Aluminium

Q.9 The damage in the ion-implanted sample is primarily due to
(a) Electronic stopping
(b) Nuclear stopping
(c) A combination of electronic and nuclear stopping
(d) None of the above

Q.10 Epitaxial growth is used in integrated circuit
(a) because it produces low parasitic capacitance
(b) because it yields back-to-back isolating junctions
(c) to grow single crystal n-doped silicon on a single-crystal p-type substrate
(d) to grow selectively single-crystal p-doped silicon of one resistivity on p -type substrate of a different resistivity.

Q.11 The photoetching process consists in
(a) remove of photoresist
(b) curbing lines on the wafer before dicing
(c) diffusing impurities
(d) removed of layer from selected portion

ANSWERS

1. (d)	2. (c)	3. (d)	4. (c)	5. (d)
6. (a)	7. (d)	8. (a)	9. (b)	10. (c)
11. (d)				

Student's Assignments 2

Q.1 An n-type silicon substrate has 0.5 lim oxide covering the entire surface area. Now 100 μm x 100 (im windows are opened in the oxide and boron is diffused through the windows. The drive-in after diffusion is carried out in an oxidizing ambient for which $B = 0.3$ lim^2/h and $A = 0.2$ um. This drive-in is continued for two hours. After this step,

(a) what is the thickness of oxide on the windows?

(b) what is the thickness of oxide elsewhere on the substrate?

Q.2 Phosphorus is diffused into silicon from an infinite source at 1000°C for 30 min.

(a) Find out the total amount of phosphorus per unit area that has gone into silicon.

(b) After step (a), the source is shut off and the sample is subjected to drive-in at 1200°C. If the final surface concentration is to be maintained at 5×10^{19} per cm^3, what should be the duration of drive-in?

(c) If the original substrate doping was 10 per cm^3, what is the junction depth after step (b)?

[Given: for phosphorus diffusion, $D_{1000} = 3 \times 10^{-14}$cm^2/s, $D_{1200} = 2.5 \times 10^{-12}$ cm^2/s, solid solubility of phosphorus at 1000°C = 10^{21} per cm^3]

Q.3 In a particular oxidation process carried out on unoxidized silicon wafers, the following data was noted:

Oxidation time (t)	Oxide thickness (d)
30 minutes	0.12 μm
60 minutes	0.20 μm

How much time will it take to grow an oxide of thickness 0.3 p:m in this process?

Q.4 Boron is implanted at 100 KeV into n-type silicon with a background concentration of 10^{15}/ cm^3.

(a) If the beam current is 1 mA and the target area is 100 cm^2, how long should the implantation be carried out to realize a dose of 4×10^{15} per cm^2?

(b) Calculate the location of the p-n junction thus formed and the peak doping concentration. Assume R_p = 3 μm/MeV and $\Delta R_p = 0.3R_p$.

(c) Sketch the doping profile after the above process.

Q.5 Windows of dimensions 5 μm × 5 lim are to be etched in an oxide layer grown on silicon substrate. Draw the mask patterns neatly if (a) positive photoresist (b) negative photoresist are to be used.

Q.6 (a) What is the principal source from which oxygen is unintentionally incorporated during Czochralski growth of silicon?

(b) By which technique is it possible to grow single crystal silicon with lower oxygen incorporation?

■■■■