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ELECTRONICS ENGINEERING

Objective Practice Sets

Computer Organization & Architecture

1
CHAPTER

Computer Organization and Architecture

Memory Organization and IO Organization

Q.1 When an interrupt occurs, an operating system
(a) ignores the interrupt
(b) always changes state of interrupted process after processing the interrupt
(c) always resumes execution of interrupted process after processing the interrupt
(d) may change state of interrupted process to 'blocked' and schedule another process

Q.2 A system uses FIFO policy for page replacement. It has 4 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur?
(a) 196 (b) 192
(c) 197 (d) 195

Q.3 If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?
(a) Width of tag comparator
(b) Width of set index decoder
(c) Width of way selection multiplexor
(d) Width of processor to main memory data bus

Q.4 According to temporal locality, processes are likely to reference pages that
(a) have been referenced recently.
(b) are located at address near recently referenced pages in memory.
(c) have been preloaded in memory.
(d) None of these

Q.5 A system which has a lot of crashes, data should be written to the disk, using
(a) Write – through
(b) Write – back
(c) Any one from (a) and (b)
(c) Some other techniques are required and none of the above can do this.

Q.6 The principle of locality justifies the use of
(a) Interrupts (b) Threads
(c) DMA (d) Cache Memory

Q.7 Consider a system with 2 level cache. Access times of level 1 cache, level 2 cache and main memory are 1 ns, 10 ns and 500 ns respectively. The hit rates of level 1 and level 2 caches are 0.8 and 0.9 respectively. What is the average access time of the system ignoring the search time within the cache?
(a) 13.0 (b) 12.8
(c) 12.6 (d) 12.4

Q.8 Consider a memory system with the following parameters :

T_c = Cache Access Time
= 100 ns
T_m = Main Memory Access Time
= 1200 ns

If we would like to have effective (average) memory access time to be or more than 20% higher than cache access time, the hit ratio for the cache must at least be :
(a) 80% (b) 90%
(c) 98% (d) 99%

Q.9 A disc drive has an average seek time of 10 ms, 32 sectors on each track and 512 bytes per sector. If the average time to read 8 kbytes of continuously stored data is 20 ms, what is the rotational speed of the disc drive?
(a) 3600 rpm (b) 6000 rpm
(c) 3000 rpm (d) 2400 rpm

Q.10 In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is
(a) Non-maskable and non-vectored
(b) Maskable and non-vectored
(c) Non-maskable and vectored
(d) Maskable and vectored

Q.11 The access time of a cache memory is 100 ns and that of main memory is 1 μs. 80% of the memory requests are for read and others are for write.

Codes:

(a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).

(b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).

(c) Statement (I) is true but Statement (II) is false.

(d) Statement (I) is false but Statement (II) is true.

Q.36 **Statement (I):** A memory module presents a specific memory interface to the processor or other unit that references memory.
Statement (II): Memory module contains buffer registers for the address and data.

Q.37 **Statement (I):** LRU (Least Recently Used) replacement policy is not applicable to direct mapped caches.
Statement (II): A unique memory page is associated with every cache page in direct mapped caches.

Q.38 **Statement (I):** Most personal computers use static RAMs for their main memory.
Statement (II): Static RAMs are much faster than dynamic RAMs.

Q.39 **Statement (I):** Associative memory is fast memory.
Statement (II): Associative memory searches by content and not by accessing of address.

■■■■

Answers Memory Organization and IO Organization

1. (d)	2. (a)	3. (d)	4. (a)	5. (a)	6. (d)	7. (a)	8. (b)	9. (b)
10. (d)	11. (b)	12. (d)	13. (d)	14. (a)	15. (a)	16. (c)	17. (a)	18. (c)
19. (d)	20. (b)	21. (b)	22. (b)	23. (b)	24. (c)	25. (a)	26. (c)	27. (a)
28. (a)	29. (b)	30. (c)	31. (c)	32. (b)	33. (b)	34. (d)	35. (a)	36. (a)
37. (d)	38. (d)	39. (a)						

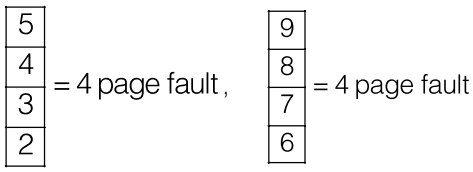
Explanations Memory Organization and IO Organization

1. (d)

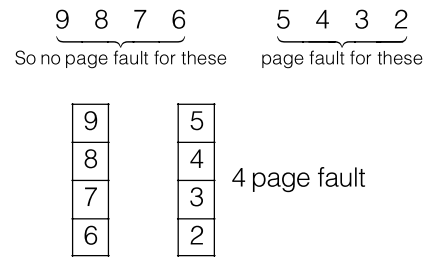
An interrupt is a signal from a device attached to a computer or from a program within the computer that causes the main program that operates the computer to stop and figure out what to do next. After the interrupt signal is sensed, it may change state of interrupted process to 'blocked' and schedule another process.

2. (a)

FIFO policy for page replacement used.
Access 100 distinct pages by taking some example: 2 3 4 5 6 7 8 9
So by loading it get



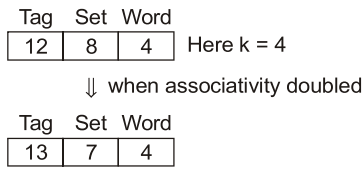
and now access these page in reverse so



So, total = 4 + 4 + 4 = 12 page fault
For 8 pages = 2 × 8 – 4 = 12
So, for n pages = 2n – 4
So, for 100 pages = 2 × (100) – 4 = 196

3. (d)

Assume,



- Since, tag bits have been changed thus width of a Tag comparator changes.
- Since, width of set bits changed thus width of a set index decoder.
- Width of multiplexor change since k changes.

4. (a)

Temporal locality says that recently executed instruction is likely to be executed very soon.

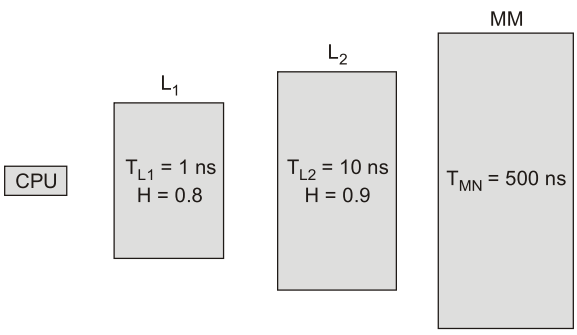
5. (a)

System which has lot of crashes, data should be written to the disk as soon as possible thus, write through cache is preferable.

6. (d)

Principle of locality states that many instruction in localized areas of the programs are executed repeatedly during short time period and the remainder of the program is accessed relatively less frequently. This is where use of cache comes into existence.

7. (a)



$T_{avg} = 0.8 \times 1 + 0.2 \times 0.9 \times (1 + 10) + 0.2 \times 0.1 \times 511$
$= 0.8 + 1.98 + 10.22 = 13$ ns

8. (b)

$$T \geq 1.2\, T_c = 120$$
$$T = H.T_c + (1 - H)(T_m)$$
$$T = H.100 + (1 - H)(1200)$$
$$T = 100H + 1300 - 1200H$$
$$T = 1200 - 1200\, H \geq 120$$
$$1200\, H = 1200 - (120)$$
$$H = \frac{1200}{1200} - \frac{(120)}{1200}$$
$$H = 1 - 0.1 = 0.9$$
$$\text{Hit Ratio} = 90\%$$

9. (b)

Average access time
= avg. seek time + avg. rotational latency + avg. transfer time

Here, for 1 round $= \frac{60\,\text{sec}}{n} = \frac{60{,}000}{n}$ msec

$\therefore$ Average rotational latency $= \frac{60{,}000}{2n}$

Also : 32×512 bytes = 1 track $= \frac{60{,}000}{n}$ msec

$\therefore$ 8 k byte $= \frac{60{,}000 \times 8 \times 2^{10}}{n \times 32 \times 512}$

$= \frac{60{,}000}{2n}$ msec

So, $\frac{60000}{2n} + \frac{60000}{2n} + 10 = 20$

$\therefore$ $n = 6000$ rpm

10. (d)

Maskable interrupt is one which can be delayed or rejected due to non-urgency when the microprocessor is busy.
If the instruction execution program is already written at a particular fixed location, then it is called vectored instruction.

11. (b)

Read access time
$= HT_c + (1 - H)(T_c + T_m)$
$= 0.9 \times 100 + 0.1 \times (100 + 1000)$nsec $= 200$ nsec.
Total access time
$= (0.8 \times 200 + 0.2 \times 1000)$nsec $= 360$ nsec.

12. (d)

Number of blocks $= \frac{4K}{64} = 64$

Number of sets $= \frac{64}{4} = 16$

$\Rightarrow$ 4 bits for SET
Each block has 64 words
$\Rightarrow$ 6-bits required for word.

Tag	Set	Word
	4-Bits	6-Bits

13. (d)

Disk is the IO device attached externally to the processor. Therefore, disk requires a device driver.

14. (a)

Number of surfaces (on which data can be stored)
$= 6 \times 2$
Each surface can hold
= Number of tracks $\times$ Number of sectors per track $\times$ Size of sector
$= 200 \times 50 \times 512$
Storage capacity $= 200 \times 50 \times 512 \times 12$ B