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CONTENTS

COMPUTER SCIENCE & IT

Objective Practice Sets

Computer Organization & Architecture

1 CHAPTER
Basics of Computer Design

Multiple Choice Questions & NAT Questions

Q.1 The computer performs all mathematical and logical operations inside its
(a) Memory unit (b) Central processing unit
(c) Output unit (d) Visual display unit

Q.2 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Pointer
B. Position Independent code
C. Constant operand

List-II
1. Indirect AM
2. Immediate AM
3. Relative AM

Code:

	A	B	C
(a)	1	2	3
(b)	3	2	1
(c)	1	3	2
(d)	2	3	1

Q.3 The most appropriate matching of the following pairs is

Column 1	Column 2
X: Indirect addressing	1. Loops
Y: Immediate addressing	2. Pointers
Z: Auto-decrement address	3. Constant

(a) X-2, Y-3, Z-1 (b) X-3, Y-2, Z-1
(c) X-1, Y-3, Z-2 (d) X-3, Y-1, Z-2

Q.4 Consider the following I/O instruction format for IBM 370 I/O channel

Operation Code	Channel Address	Device Address

Then operation code specifies
1. Test I/O
2. Test channel
3. Store channel identification
4. Halt device

(a) Only 1 and 4 (b) Only 2 and 3
(c) 1, 2, 3 and 4 (d) Only 1, 3 and 4

Q.5 An interrupt that can be temporarily ignored by the counter is known as
(a) Vectored interrupt
(b) Non-maskable interrupt
(c) Maskable interrupt
(d) Low priority interrupt

Q.6 A processor can support a maximum memory of 4 GB where memory is word addressable and word is 2 bytes. What will be the size of the address bus of the processor?
(a) At least 2 bytes (b) At least 28 bits
(c) At least 31 bits (d) Minimum 4 bytes

Q.7 A digital computer has memory unit with 24 bits word. The instruction set consists of 150 different operations. All instructions have an operation code part and an address part. Each instruction is stored in one word of memory. How many bits are needed for the OPCODE and how many bits are left for the address of the instruction.
(a) 8, 16 (b) 16, 64
(c) 4, 8 (d) 8, 64

Q.8 An instruction is stored at location 300 with its address field. At location 301 the address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address matching the following addressing modes to their respective addresses.

A. Direct	1. 702
B. Immediate	2. 200
C. Relative	3. 400
D. Register indirect	4. 600
E. Index (R1 is index)	5. 301

(a) A3 B5 D2 E4 C1 (b) A3 B4 C1 D1 E5
(c) A5 B3 C2 D1 E4 (d) A4 B3 C1 D5 E2

Q.75 The format of double operand instruction of a CPU consist of 5 bits opcode and 6 bits for source and destination. 26 double operand instructions and 184 single operand instructions must be implemented. What will be the total number of zero operand instructions can be implemented?
(a) 819200
(b) 409600
(c) 12800
(d) None of these

Q.76 Consider the hypothetical processor which has 256 words memory. A 19 bits instruction is placed in 1 memory cell. It supports 2-address, 1-address and 0-address instructions. It uses expanding opcode technique. If there exist five 2-address instructions and 760 1-address instructions, then number of 0-address instructions are _____.

Q.77 In a certain processor a 4 byte jump instructions is encountered at memory address 2014. Jump instruction is in PC relative mode. The instruction is JMP–10 (where –10 is signed byte).
What is the branch target address?
(a) 2010 (b) 2004
(c) 2006 (d) 2008

Multiple Select Questions (MSQ)

Q.78 A certain architecture supports indirect, direct and register addressing modes for use in identifying operands for arithmetic instructions. Which of the following can be achieved with a single instruction?
(a) Specifying a register number in the instruction such that the register contains the value of an operand that will be used by the operation.
(b) Specifying a register number in the instruction such that the register will serve as the destination for the operands output.
(c) Specifying an operand value in the instruction such that the value will be used by the operation.
(d) Specifying a memory location in the instruction such that the memory location contains the value of an operand that will be used by the operation.

Q.79 A machine has 24 bit instruction format. It has 32 registers and each of which is 32 bit long. It needs to support 49 operation. Each instruction has two register operands and one immediate operand. Which of the following are correct?
(a) Total 5 bits are needed for opcode.
(b) The minimum value of immediate operand is –256 if operand is signed integer.
(c) The minimum value of immediate operand is –127 if operand is signed integer.
(d) The maximum value of immediate operand is 255 if operand is signed integer.

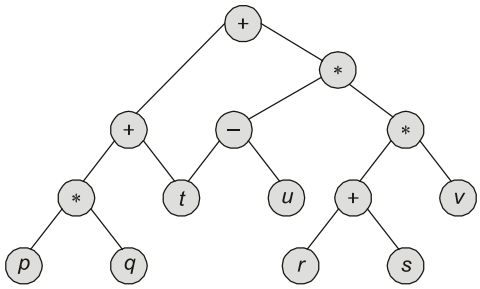
Q.80 Consider a hypothetical system which has 32 bit instruction size and 8 bit address. If there are 180 2-address instructions and 400 one 1-address instruction then which of the following are correct?
(a) Total opcodes possible is 2^{12}.
(b) Number of 1-address instruction $= (2^{16} - 180) \times 2^8$
(c) Number of zero-address instruction $= ((2^{16} - 180) \times 2^8 - 400) \times 2^8$
(d) Number of zero-address instruction $= (2^{16} - 180 \times 2^8 - 400) \times 2^8$

Q.81 Consider a 16 bit hypothetical CPU which supports 2-word instruction with 1 register operand 1 memory operand and 8 bit immediate constant field. CPU instruction size is 48 and register file size is 22. Which of the following statements are incorrect?
(a) Main memory size is 16 KB
(b) Opcode size is of 6 bit
(c) Register size is 4 bit
(d) Main memory size is 8 KB

Q.82 Consider a system with instruction set that uses a fixed 16 bit instruction length and length of address is 6 bits. There are 10 2-address instruction and 8192 zero-address instructions. Which of the following are correct?
(a) Maximum 512 zero-address instructions can be supported in the system.
(b) Maximum 256 1-address instructions can be supported in the system.
(c) Maximum 8192 zero address instructions can be supported in the system.
(d) Maximum 64 1-address instructions can be supported in the system.

Q.83 Consider the evaluation of following expression tree on a machine in which memory can be accessed only through load and store instructions. The variable *p*, *q*, *r*, *s*, *t*, *u* and *v* are initially stored

in memory. The binary operators used in the tree can be evaluated by the machine only when all operands are in register. The instruction produce result only in a register.



What is the minimum number of registers needed to evaluate the expression if, no intermediate results can be stored in memory?

(a) 3 (b) 4
(c) 5 (d) 6

■■■■

Answers Basics of Computer Design

1.	(b)	2.	(c)	3.	(a)	4.	(c)	5.	(c)	6.	(c)	7.	(a)	8.	(a)	9.	(a)
10.	(c)	11.	(b)	12.	(a)	13.	(c)	14.	(c)	15.	(c)	16.	(d)	17.	(d)	18.	(369)
19.	(16383)	20.	(b)	21.	(b)	22.	(d)	23.	(c)	24.	(b)	25.	(b)	26.	(3009)	27.	(d)
28.	(d)	29.	(b)	30.	(c)	31.	(62)	32.	(c)	33.	(d)	34.	(d)	35.	(b)	36.	(c)
37.	(b)	38.	(c)	39.	(d)	40.	(b)	41.	(c)	42.	(b)	43.	(c)	44.	(d)	45.	(d)
46.	(c)	47.	(c)	48.	(a)	49.	(a)	50.	(c)	51.	(a)	52.	(c)	53.	(b)	54.	(a)
55.	(–128)	56.	(a)	57.	(a)	58.	(b)	59.	(d)	60.	(a)	61.	(d)	62.	(16)	63.	(d)
64.	(b)	65.	(c)	66.	(a)	67.	(d)	68.	(92)	69.	(2032)	70.	(c)	71.	(a)	72.	(b)
73.	(c)	74.	(b)	75.	(c)	76.	(2048)	77.	(d)	78.	(a, b, d)	79.	(c)	80.	(b, c)		
81.	(a, c)	82.	(b, c)	83.	(b)												

Explanations Basics of Computer Design

2. (c)

For making use of pointer in programs, indirect addressing mode is used.

Pointer stores the address of a variable and indirect addressing mode stores address of effective address the instruction.

Position independent code make use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.

Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

4. (c)

The operation code specifies one of eight input output instructions: Start input/output, start input/output fast release, test input/output, clear input/output, halt input/output, halt device, test channel and store channel identification.

5. (c)

Maskable interrupt temporally ignored by counter.

6. (c)

Memory size = 4 GB = 2^{32} B

Word size = 2 B

So, unique address = $\frac{2^{32}}{2^1} = 2^{31}$

Hence, atleast 31 bits are required.

7. (a)

Each instruction is stored in one word of memory. Memory is word addressable and 1 word = 24 bits ⇒ 3 bytes.

Total number bits = 24

The instruction set consists of 150 different operations. To generate 150 different operations we need minimum 8 bits are required.

OP code	Address
8	16

So, option (a) is correct.

8. (a)

For direct, EA = address field value in IR (instruction register) = 400

For immediate, actually no meaning of effective address. So, EA here will be just the address of the operand field which is otherwise address field = 301.

For relative addressing, we have EA = PC value (current) + Address field value

EA = 302 + 400 = 702

For register indirect, the EA is the content of the register, the register name being present in the address field of instruction.

So, EA = content of R1 = 200

For indexed mode = Base address + index register content

= 400 + 200 = 600

So, option (a) is correct.

10. (c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

So, option (c) is correct.

11. (b)

- Stack over flow is a internal interrupt.
- Supervisor call is a software interrupt.
- Invalid opcode is a internal interrupt.
- Timer is a external interrupt.

12. (a)

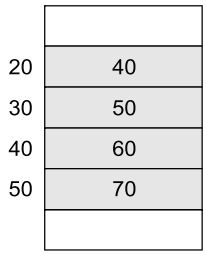
The Jump instruction is at address 3010 H and instruction is 2 bytes. Therefore, PC points to 3012 H on execution of this instruction.

Now Branch Target PC = PC + (–7)

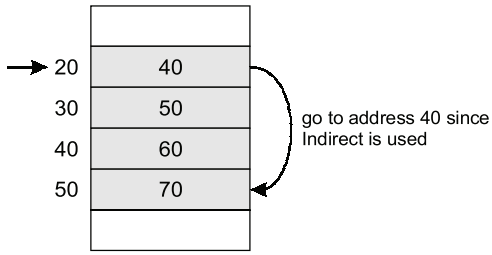
= 3012 H – 7 H = 300 BH

14. (c)

The given information can be understood as



Now load indirect 20 will load 60 into as follows



Hence (c) is correct option.

16. (d)

In immediate addressing mode, the operand is specified in the instruction itself.

For example: MOV R1, 12H is the immediate AM with 12 is operand.

17. (d)

$$\begin{array}{r} 00000010 \\ 00000011 \\ \hline 00000101 \end{array}$$

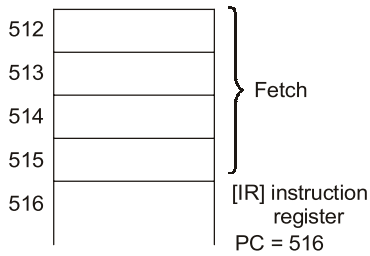
Overflow = 0, sign = 0, half carry = 0

Half carry indicate addition of pack at decimal numbers. When carry takes out of the lower digit order, this flag is set.

Auxiliary carry is also known as half carry.

18. (369)

4 byte instruction storage



Effective address = PC + Relative value

Relative value = EA – PC

= 885 – 516 = (369)10

So, answer is 369.

2 CHAPTER

CPU Design

Multiple Choice Questions & NAT Questions

Q.1 The Ionic features of the RISC machine among the following are
(a) Reduced number of addressing modes
(b) Having branch delay slot
(c) Increase memory size
(d) All of the above

Q.2 What is not true about RISC?
(a) It used for real time application.
(b) It uses hardwired control unit.
(c) Instruction cannot be completed in one machine cycle.
(d) It is a type of microprocessor that has a limit number of instructions.

Q.3 Which processor has the necessity of manual optimization for the generation of assembly language code especially for the embedded system?
(a) RISC (b) CISC
(c) Both (a) and (b) (d) None of these

Q.4 Which statement is false in case of microprogram control?
(a) In a microprogram control, the control variables that initiate micro-operations are stored in memory. The control memory is usually a ROM, since the control sequence is permanent and needs no alternation
(b) The control variables stored in memory are read one at a time to initiate the sequence of micro-operations for the system
(c) The words stored in a control memory are micro instructions, and each micro instruction specifies one or more micro-operations for the components in the system
(d) Once these micro-operations are executed, the control unit must determine its next address. Therefore, all bits of the micro instruction are used to control the generation of the address for the next micro instruction

Q.5 The bus system of a machine has the following propagation delay times: 40 ns for the signals to propagate through the multiplexers, 90 ns to perform the ADD operation in the ALU, 30 ns delay in the destination decoder, and 20 ns to store the data into the destination register. What is the minimum cycle time that can be used for the clock?
(a) 120 ns (b) 150 ns
(c) 160 ns (d) 180 ns

Q.6 Which set of instruction transfers the memory word specified by the effective address to AC or Load to AC?
(a) $DR \leftarrow M[AR]$
$AC \leftarrow AC + DR, E \leftarrow C_{out}, SC \leftarrow 0$
(b) $DR \leftarrow M[AR]$
$AC \leftarrow DR, SC \leftarrow 0$
(c) $M[AR] \leftarrow AC, SC \leftarrow 0$
(d) $DR \leftarrow M[AR]$
$AC \leftarrow AC \wedge DR, SC \leftarrow 0$

Q.7 Suppose a processor does not have any stack pointer registers, which of the following statements is TRUE?
(a) It cannot have subroutine call instruction
(b) It can have sub routing call instruction, but no nested subroutine calls
(c) Nested subroutine calls are possible, but interrupts are not.
(d) All sub routing calls and interrupts are possible.

Q.8 Assume that the control memory is 30 bits wide. The microinstruction format is divided into 3 fields. A micro operation field of 15 bits specifies the micro-operations to be performed. An address selection field specifies a condition based on flags and control memory address field. There are 8 flags. How many bits are there in address selection field, address field and what is the size of control memory in words respectively?

(a) 2, 12, 2048 (b) 2, 10, 2048
(c) 3, 12, 4096 (d) 3, 10, 1024

Q.9 In a register/memory type CPU, the instruction lengths are typically variable. This presents a problem when the program counter (PC) of the CPU is incremented during the fetch-execute cycle. Which statements is/are true with regard to PC incrementing?

(a) PC is incremented by the largest possible fixed value, irrespective of the variability.
(b) Increment value is known when the current instruction is decoded within the IR.
(c) Increment value is known when the current instruction has completed execution.
(d) The binary loader overcomes the problem by positioning instructions at word boundaries so that PC can be incremented by a constant amount.

Q.10 What is the control unit's function in the CPU?

(a) To decode program instructions.
(b) To transfer data to primary storage.
(c) To perform logical operations.
(d) To store program instructions.

Q.11 Which of following registers processor used for fetch and execute operations?

1. Program counter
2. Instruction register
3. Address register

(a) 1 and 3
(b) 1 and 2
(c) 2 and 3
(d) 1, 2 and 3

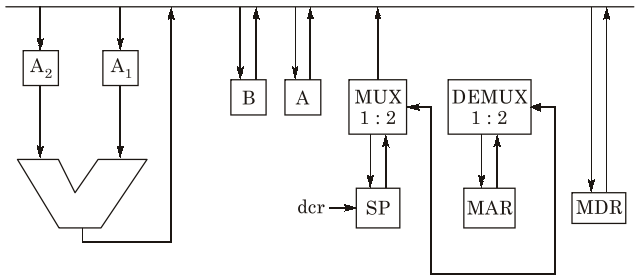
The processor used program counter and instruction register for fetch and execute operations.

Q.12 Microinstruction length is determined by _____.

1. The maximum number of simultaneous micro operations that must be specified.
2. The way in which the control information is represented or encoded.
3. The way in which the next microinstruction address is specified.

(a) 1 and 2
(b) 2 and 3
(c) 1 and 3
(d) All of these

Q.13 Consider the following data path of a simple non-pipelined CPU. The registers A, B, A_1, A_2, MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size 8 × (2 :1) and the DEMUX is of size 8 × (1:2). Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Data Register). SP can be decremented locally.



The CPU instruction "push r", where r = A or B, has the specification

M [SP] ← r
SP ← SP – 1

How many CPU clock cycles are needed to execute the "push r" instruction?

(a) 2 (b) 3
(c) 4 (d) 5

Q.14 Determine the width of Micro-instruction having following Control signal field, in a Vertical Micro-programmed Control Unit

1. Next Address field of 7 Bits
2. ALU Function field selecting 1 out of 13 ALU Function.
3. Register-in field selecting 1 out of 13 ALU Function.
4. Register-out field selecting 1 out of 8 registers.
5. Shifter field selecting no shift, right shift or left shift.
6. Auxiliary control field of 4 bits.

(a) 22 (b) 23
(c) 24 (d) 25

Q.15 Find the memory address of the next instruction executed by the microprocessor (8086), when operated in real mode for CS = 1000 and IP = E000

(a) 10E00 (b) 1E000
(c) F000 (d) 1000E

Q.45 Which of the following statement are correct?

(a) Address decoder is an essential part of I/O interface.

(b) Compared to RISC processor CISC processor contains large instruction set and less number of registers.

(c) Separate I/O address space does not necessarily mean that I/O address lines are physically separated.

(d) None of these

Q.46 Consider the following Booth's multiplication:

Multiplicand: 1011 0111 1111

Multiplier: 0110 1001 0110

How many arithmetic operations (excluding shift operations) are required in the multiplication.

(a) 6 (b) 7

(c) 8 (d) 9

■■■■

Answers CPU Design

1.	(b)	**2.**	(c)	**3.**	(b)	**4.**	(d)	**5.**	(b)	**6.**	(b)	**7.**	(a)	**8.**	(c)	**9.**	(c)
10.	(a)	**11.**	(b)	**12.**	(d)	**13.**	(a)	**14.**	(b)	**15.**	(c)	**16.**	(415)	**17.**	(c)	**18.**	(c)
19.	(a)	**20.**	(5)	**21.**	(d)	**22.**	(c)	**23.**	(d)	**24.**	(b)	**25.**	(c)	**26.**	(a)	**27.**	(c)
28.	(b)	**29.**	(d)	**30.**	(a)	**31.**	(c)	**32.**	(94)	**33.**	(a)	**34.**	(d)	**35.**	(b)	**36.**	(a)
37.	(a)	**38.**	(b)	**39.**	(c)	**40.**	(a)	**41.**	(a, b, c)	**42.**	(a, b, c)	**43.**	(a, b, c)				
44.	(b)	**45.**	(a, b, c)	**46.**	(c)												

Explanations CPU Design

1. (b)

Having branch delay slot is iconic feature of RISC machine.

A branch delay slot is an instruction space immediately following a jump or branch. When a branch instruction is involved the location of the following delay slot instruction in the pipeline may be called a branch delay slot. Branch delay slot are found mainly in order RISC architecture and DSP architecture.

2. (c)

RISC is hardwired and instruction take single clock cycle to get executed.

3. (b)

CISC has many specified instructions, some of which may only be rarely used in practical programs thus has a necessity of manual optimization for the generation of assembly language code especially for the embedded systems.

5. (b)

(40 + 90 + 20) = 150 ns

Selection of destination register that takes 30 ns can be done parallelly with other operations.

6. (b)

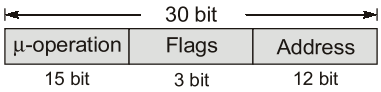
LDA AC load to AC instruction transfers the memory word specified by the effective address to AC

T_1 : MDR ← M[AR]
T_2 : AC ← MDR, SC ← O
Here register MD represent MDR.

7. (a)

Stack pointer register hold the address of top of stack, which is the location of memory at which CPU should resume its execution after serving some interrupt or sub routing call.
So, if SP register is not available then no subroutine call instructions are possible.
So, option (a) is correct.

8. (c)



CM size = 2^{12} CW = 4096 CW

11. (b)

The processor used program counter and instruction register for fetch and execute operations.

13. (a)

SP is decremented locally.
Therefore memory operation needs 2 clocks.

14. (b)

Next Address Field = 7 Bits
ALU Function Field is of 4 Bits (to select possible 1 of 13 ALU function)
Register-in and Register-out Fields of 3 Bits each
Shifter Field of 2 bits to select 1 out of three possibilities.
Auxiliary Field of 4 Bits
Total Bits in μ-instruction

= 7 + 4 + 3 + 3 + 2 + 4 = 23

15. (c)

In 8086 the address bus is 20 bit. The address is generated by using segment base and offset.
i.e. Address = segment *0x10 + Offset (Here segment is multiplied by 10 h)
Given: Segment base (CS) - 0 x1000 and Offset (IP) = 0xE000
Therefore,

Addresses = CS*0x10 + IP
= 0x1000*0x10 + 0xE000
= 0x1E000

16. (415)

The address allocation can be given as:

Instruction	Address location
MOV r_0, @ 2000	400
MOV r_1, 3 (r_0)	404
Add r_0, [2000]	407
MUL [3000], r_0	409
MOV @ 2000, r_1	411
Halt	415

When halt is executing, the value of PC will be 415, then return address will be 415.

18. (c)

Since PLA is neither a hard-wired model nor a memory.
∴ We can say control unit with PLA as Hard-wired or micro programmed control unit.

20. (5)

Since, none or one control signal is active at a time it is the case of vertical programming.
Number of bits required to generate control signals

= $\log_2(25) = 5$

21. (d)

None or one of 6 micro-instructions is one kind (vertical μ-instruction) = $\log_2 6$ bits = 3 bits
Atmost 6 μ-operation = 6 bits (horizontal μ-instruction)

Total = 3 + 6 = 9 bits

22. (c)

We have to design 16 K bytes memory or
We can say 16 K × 8 bit memory (∵ 1 byte = 8 bit) word.
Length of chip is = 12 + 4 = 16 = 2^4
∴ bits required per chip = 4 bits
Hence, total line of memory chips is

= 2^{12} × 4 bits
$2^{12} \times 4 = 2^{12} \times 22 = 2^{14}$
= 16 K bits

Mean size of memory chip is 16 K bits.
Now, we have to find how many chips of 16 K bits can be constructed using 16 K × 8 bits memory.

∴ Number of chips = $\frac{16\text{ K} \times 8\text{ bit}}{16\text{ K bit}} = 8$ chips

3 CHAPTER

Instruction Pipelining

Multiple Choice Questions & NAT Questions

Q.1 Pipelining improves CPU performance due to
(a) Reduced memory access time
(b) Increased clock speed
(c) The introduction of parallelism
(d) Additional functional units

Q.2 An instruction cycle refers to
(a) Fetching an instruction
(b) Clock speed
(c) Fetching, decoding and executing an instruction
(d) Executing an instruction

Q.3 The performance of a pipelined processor suffers if
(a) The pipeline stages have different delays.
(b) Consecutive instructions are dependent on each other.
(c) The pipeline stages share hardware resources.
(d) All of the above

Q.4 What will be the efficiency (in percentage) of the pipeline if 5 stage pipelined with the respective delay of 20, 30, 40, 50, 60?

Q.5 An instruction cycle refers to
(a) Fetching an instruction
(b) Clock speed
(c) Fetching, decoding and executing an instruction
(d) Executing an instruction

Q.6 A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be
(a) 120.4 ms (b) 160.5 ms
(c) 165.5 ms (d) 590.0 ms

Q.7 Pipelining is an implementation technique where multiple instructions are overlapped in execution. What among the given is the function of the pipeline.
(a) Increase the length of machine cycle
(b) Decrease the individual instruction execution time.
(c) Increase the instruction throughput
(d) None of these

Q.8 Assume the individual stages of the data path have the following latencies.

Instruction decode (ID): 8 ns
Execution (EX) : 6 ns
Memory (MEM) : 9 ns
Write back (WB) : 5 ns

Find the clock cycle time (in ns) in a non-pipelined (single cycle) processor.
(a) 40 (b) 60
(c) 35 (d) 45

Q.9 Pipelining is an implementation technique where multiple instructions are overlapped in execution. What among the given is the function of the pipeline.
(a) Increase the length of machine cycle.
(b) Decrease the individual instruction execution time.
(c) Increase the instruction throughput
(d) None of these

Q.10 The performance of a pipelined processor suffers if
(a) the pipeline stages have different delays
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) All of the above

Q.11 Assume the individual stages of the data path have the following latencies.

Instruction Fetch (IF) : 10 ns
Instruction Decode (ID) : 8 ns
Execution (EX) : 6 ns
Memory (MEM) : 9 ns
Write Back (WB) : 5 ns

Find the clock cycle time in a non-pipelined (single cycle) processor?

(a) 10 ns (b) 18 ns
(c) 28 ns (d) 38 ns

Q.12 Consider the following instructions:

I_1: $R_1 = 100$
I_2: $R_1 = R_2 + R_4$
I_3: $R_2 = R_4 + 25$
I_4: $R_4 = R_1 + R_3$
I_5: $R_1 = R_1 + 30$

Calculate sum of (WAR, RAW and WAW) dependencies the above instructions.

(a) 10 (b) 12
(c) 7 (d) 8

Q.13 Consider a pipelined system with four stages: IF, ID, EX, WB. Following chart shows the clock cycles required by each instruction to complete each stage.

Instructions	Instruction Fetch (IF)	Instruction Decode (ID)	Instruction Execute (EX)	Write Back (WB)
I_0	1	1	2	1
I_1	2	2	3	1
I_2	2	2	2	2
I_3	2	1	1	1
I_4	3	2	1	2

How many clock cycles are required to complete the above instructions?

(a) 16 (b) 9
(c) 14 (d) 13

Q.14 Consider the unpipelined machine with 10 ns clock cycles. It uses four cycles for ALU operations and branches, whereas five cycles for memory operations. Assume that the relative frequencies of there operations are 40%, 20%, 40% respectively. Suppose that due to clock skew and setup, pipelining the machine adds 1 ns overhead to the clock. How much speed up in the instruction execution rate will we gain from a pipeline?

(a) 5 times (b) 8 times
(c) 4 times (d) 4.5 times

Q.15 Consider a hypothetical processor operating on 500 MHz frequency which uses different operand accessing mode described below:

Operand Fetching Mode	Frequency (%)
Indirect addressing mode	25
Direct addressing mode	30
Register addressing mode	20
Register indirect addressing mode	15
Indexed addressing mode	10

Consider the following data regarding different operations performed:

Operation	No. of cycle needed
Memory Reference (MR)	8
ALU operation (ALU)	4
Register Reference (RR)	0

The average operand fetch rate of CPU is _____ MIPS.

(a) 40.8 (b) 56.8
(c) 60.8 (d) 58.7

Q.16 Consider the following sequence of instructions:

1. LOAD F4, 16(R2)
2. LOAD F6, 48(R2)
3. MUL F10, F4, F8
4. Add F8, F10, F6
5. STORE F8, O(R3)

The number of stalls cycles during the execution of these instructions on the regular 5 stage pipelined processor is _____ (Assume that the pipeline stages are IF, ID, EX, MEM, WB).

Q.17 We have two designs D_1 and D_2 for a synchronous pipeline processor. D_1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D_2 has 8 pipeline stages each with 2 nsec execution time. How much time can be saved using design D_2 over design D_1 for executing 100 instructions?

(a) 214 nsec (b) 202 nsec
(c) 86 nsec (d) 200 nsec

Q.18 Suppose that in 1000 memory references there are 150 misses in first level and 100 miss in second level cache. Assume that miss penalty from L_2 cache to memory is 120 cycles. The hit time of L_2 cache is 50 cycles.
If there are 4 memory references per instruction, the average stall per instruction is _____.

Answers Instruction Pipelining

1.	(c)	**2.**	(c)	**3.**	(d)	**4.**	(67)	**5.**	(c)	**6.**	(c)	**7.**	(c)	**8.**	(a)	**9.**	(c)
10.	(d)	**11.**	(d)	**12.**	(c)	**13.**	(a)	**14.**	(c)	**15.**	(b)	**16.**	(5)	**17.**	(b)	**18.**	(78)
19.	(d)	**20.**	(28)	**21.**	(c)	**22.**	(0.083)	**23.**	(d)	**24.**	(219)	**25.**	(a)	**26.**	(a)	**27.**	(d)
28.	(d)	**29.**	(b)	**30.**	(a)	**31.**	(b)	**32.**	(1.27)	**33.**	(64)	**34.**	(c)	**35.**	(a)	**36.**	(c)
37.	(a)	**38.**	(d)	**39.**	(a)	**40.**	(d)	**41.**	(c)	**42.**	(c)	**43.**	(b)	**44.**	(185.74)		
45.	(b)	**46.**	(c)	**47.**	(c)	**48.**	(b)	**49.**	(3.87)	**50.**	(b)	**51.**	(22.2)	**52.**	(0.859)	**53.**	(4)
54.	(b)	**55.**	(b)	**56.**	(50)	**57.**	(6.75)	**58.**	(0.933)	**59.**	(a, c, d)	**60.**	(b, d)	**61.**	(b, c, d)		
62.	(a, b, c)																

Explanations Instruction Pipelining

1. (c)

In pipelining, a number of functional units are employed in sequence to perform a single computation.

3. (d)

The performance of a pipelined processor depends upon delays of different stage and its hardware resources also it depends upon consecutive instructions format.

4. (67)

Pipeline with 5 stages

$$K = 5, \quad \text{Max delay} = 60$$

$$\eta(\text{efficiency}) = \frac{5}{K} = \frac{200}{60}$$

$$\eta = 3.33$$

$$\eta = \frac{5}{K} = \frac{2.83}{5} = 0.67$$

67% efficiency

5. (c)

An instruction cycle is the basic operational process of a computer. It is the process by which a computer retrieves a program instruction from its memory, determines what actions the instruction dictates and carries out those actions. Also called as fetch, decode-execute cycle.

6. (c)

K stage pipeline can process n tasks in T_K time

$$T_K = [K + (n-1)]\, t$$

When $\tau = \tau_m + d$ where τ_m is the maximum stage delay so max (150, 120, 160,140) = 160

$$\tau = 160 + 5 = 165 \text{ ns}$$

$$\tau = 165 \times 10^{-3} \text{ ms}$$

$$K = 4,\ n = 1000$$

$$T = [4 + (1000 - 1)]\tau$$

$$= 1003 \times 165 \times 10^{-3} = 165.5 \text{ ms}$$

7. (c)

The throughput of the instruction pipeline is determined by how often an instruction exists the pipeline or the number of instructions that can be executed in a unit of time and this is the function of pipeline.

8. (a)

Clock cycle time = 12 + 8 + 6 + 9 + 5

= 40 ns (non-pipelined)

9. (c)

Function of pipelining is to make cycle per instruction = 1 first, for that instructions are overlapped and hence the instruction throughput is increased.

10. (d)

If the pipeline stages have different delay, then the maximum of all the delays is taken for every stage. If consecutive instruction are dependent on each other or if the pipeline stages share hardware resources, it will create stalls.

Hence all the condition will lead to an impact on the performance of pipelined processor.