COMPUTER SCIENCE & INFORMATION TECHNOLOGY

Computer Organization and Architecture

Comprehensive Theory
with Solved Examples *and* Practice Questions

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Computer Organization & Architecture

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Computer Organization and Architecture

Computer Organization and Architecture

Goal of the Subject

Basic understanding of computer organization includes:

- Understanding roles of processors, main memory, and input/output devices.
- Understanding the concept of programs as sequences of machine instructions.
- Understanding the relationship between assembly language and machine language; development of skill in assembly language programming;
- Understanding the relationship between high-level compiled languages and assembly language.
- Understanding arithmetic and logical operations with integer operands, floating-point number systems and operations.
- Understanding simple data path and control designs for processors, memory organization, including cache structures and virtual memory schemes.

Computer Organization and Architecture

INTRODUCTION

In this book we tried to keep the syllabus of Computer Organization around the GATE syllabus. Each topic required for GATE is crisply covered with illustrative examples and each chapter is provided with Student Assignment at the end of each chapter so that the students get the thorough revision of the topics that he/she had studied. This subject is carefully divided into eight chapters as described below.

1. Basics of Computer Design: In this chapter we discuss the Computer System, Data storage in the memory and Machine instructions
2. CPU Design: In this chapter we discuss the Datapath and Control unit design first is hardwired control unit second is microprogrammed.
3. Instruction Pipelining: In this chapter we discuss Performance, Instruction processing, Pipeline design and issue, Pipeline hazards, Pipeline performance analysis and Speedup.
4. Memory Hierarchy Design: In this chapter we discuss Primary memory, Associative memory, Address space and Cache memory design.
5. Input-Output and Secondary Storage: In this chapter we discuss Interface design, Input-output mode and Secondary memory.
6. Data Representation: In this chapter we discuss the Fixed and floating point formate, IEEE floating - point number representation, Computer arithmetic, Adding 2's complement numbers and Multiplying floating-point numbers.

■■■■

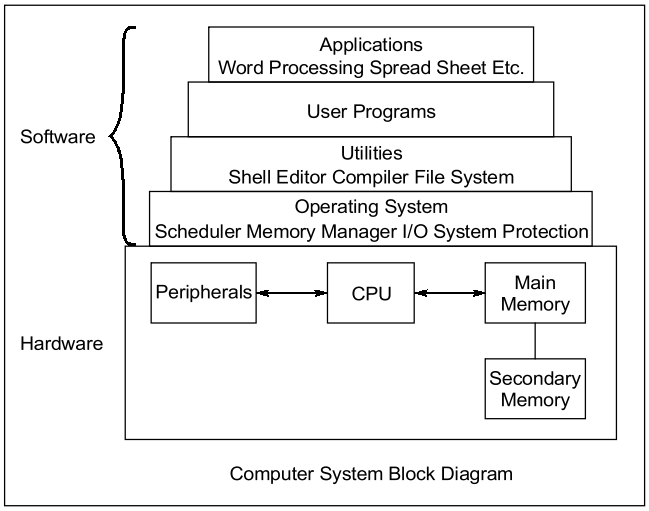
CHAPTER

1

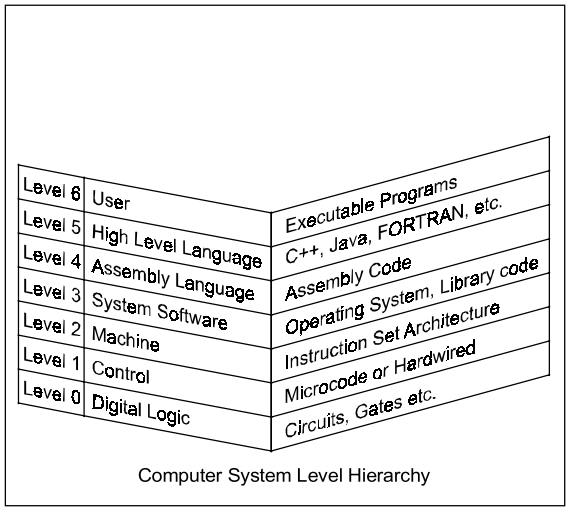
Basics of Computer Design

1.1 COMPUTER SYSTEM

Computer system is divided into two functional entities: Hardware and Software.



Computer System Block Diagram



Computer System Level Hierarchy

- **Hardware:** Lowest level in a computer are all the electronic circuits and physical devices from which it is built.

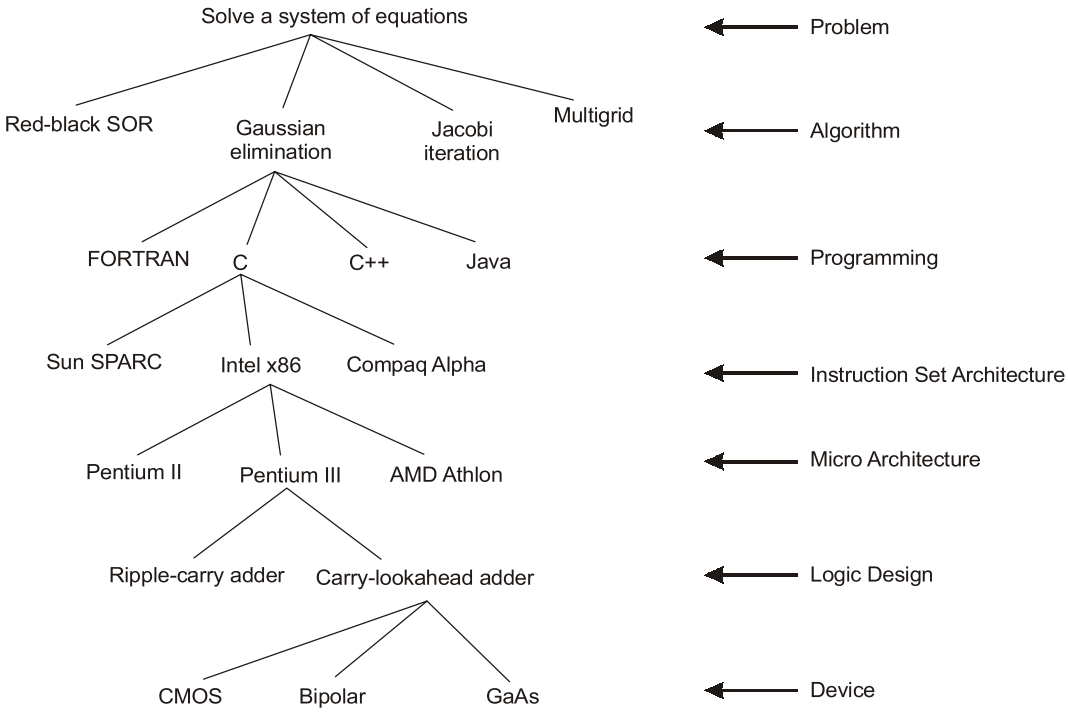
  Hardware consisting of its physical devices (CPU, memory, bus, storage devices, ...)
- **Software:** Sequences of instructions and data that make computers do useful work.

  Software, consisting of the programs it has (Operating system, applications, utilities, ...)

  Program is a sequence of instructions for a particular task.
- Operating system is set of programs included in system software package and Link between hardware and user needs.

1.1.1 Layers of Abstraction

- **Problem Statement:** stated using "natural language". It may be ambiguous are imprecise.
- **Algorithm:** step-by-step procedure, guaranteed to finish. It is definiteness, effective computability, and finiteness.
- **Program:** Express the algorithm using a computer language such as high-level language and low-level language.
- **Instruction Set Architecture (ISA):** It specifies the set of instructions the computer can perform using data types and addressing modes.
- **Micro-architecture:** It is detailed organization of a processor implementation.
- **Logic Circuits:** Combine basic operations to realize micro-architecture.
- **Devices:** Which is properties of materials and manufacturability.



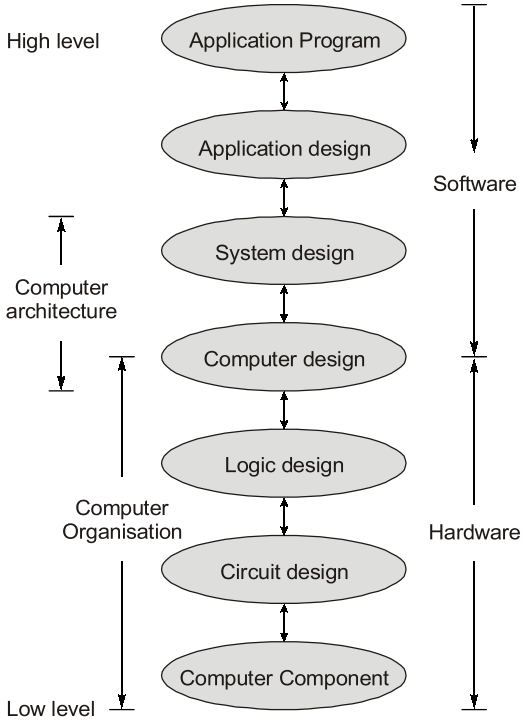
Layers of Abstraction

1.1.2 Computer Organization and Computer Architecture

Computer design: The determination of how to interconnect the components and which components to used based upon some specifications.

1.1.3 Computer Architecture (CA)

- Computer architecture is the conceptual design and fundamental operational structure of a computer system. It is a functional description of requirements and design implementations for the various parts of a computer.
- It is the science and art of selecting and interconnecting hardware components to create computers that meet functional, performance and cost goals.
- It deals with the architectural attributes like physical address memory, CPU and how they should be designed and made to coordinate with each other keeping the goals in mind.



Computer System

1.1.4 Computer Organization (CO)

- Computer architecture comes before computer organization.
- Computer organization is how operational attributes are linked together and contribute to realise the architectural specifications.
- It encompasses all physical aspects of computer systems e.g. Circuit design, control signals, memory types.

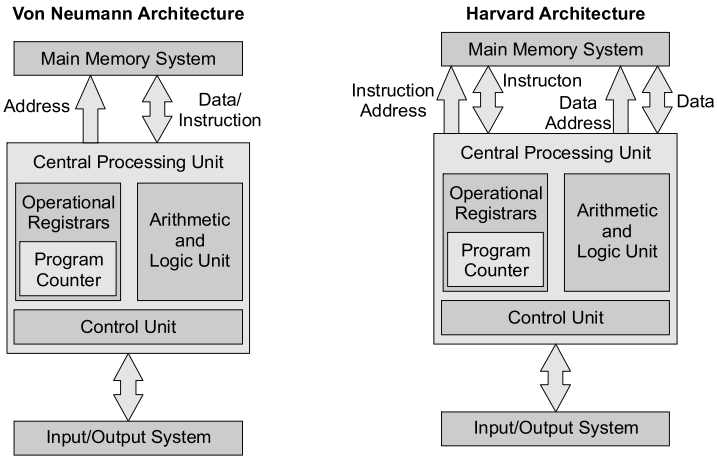
1.1.5 Computer Architecture Vs Computer Organization

Architecture and organization are independent, you can change the organization of a computer without changing its architecture.

1. The architecture indicates its hardware whereas the organization reveals its performance.
2. For designing a computer, its architecture is fixed first and then its organization is decided.

Computer Organization	Computer Architecture
• Computer organization deals with structural relationships that are not visible to the programmer (like clock frequency or the size of the physical memory).	• Computer architecture deals with the functional behavior of a computer system as viewed by a programmer (like the size of a data type – 32 bits to an integer).
• A computer's organization expresses the realization of the architecture.	• A computer's architecture is its abstract model and is the programmer's view in terms of instructions, addressing modes and registers.
• Organization describes how it does it.	• Architecture describes what the computer does.

Von-Neumann Architecture Vs Harvard Architecture



1.1.6 Evolution of Digital Computers

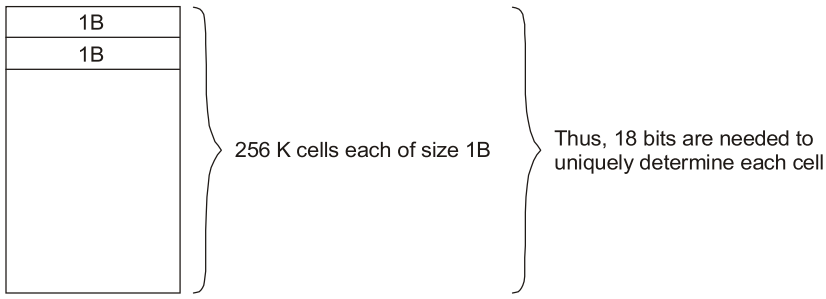
First generation: Vacuum tube computers (1945~1953)	**Second generation:** Transistorized computers (1954~1965)
• Program and data reside in the same memory (stored program concepts: John von Neumann). • Vacuum tubes were used to implement the functions (ALU & CU design). • Magnetic core and magnetic tape storage devices are used. • Using electronic vacuum tubes, as the switching components. • Assembly level language is used.	• Transistor were used to design ALU & CU. • High Level Language is used (FORTRAN). • To convert HLL to MLL compiler were used. • Separate I/O processor were developed to operate in parallel with CPU, thus improving the performance. • Invention of the transistor which was faster, smaller and required considerably less power to operate.
Third generation: Integrated circuit computers (1965~1980)	**Fourth generation:** Very large scale integrated (VLSI) computers (1980~2000)
• IC technology improved. • Improved IC technology helped in designing low cost, high speed processor and memory modules. • Multiprogramming, pipelining concepts were incorporated. • DOS allowed efficient and coordinate operation of computer system with multiple users. • Cache and virtual memory concepts were developed. • More than one circuit on a single silicon chip became available.	• CPU termed as microprocessor • INTEL, MOTOROLA, TEXAS, NATIONAL semiconductors started developing micro-processor. • Workstations, microprocessor (PC) and Notebook computers were developed. • Interconnection of different computer for better communication LAN, MAN and WAN. • Computational speed increased by 1000 times. • Specialized processors like Digital Signal Processor were also developed.
Fifth generation: System-on-chip (SOC) computers (2000~)	
• E-Commerce, E- banking, home office. • ARM, AMD, INTEL, MOTOROLA. • High speed processor - GHz speed. • Because of submicron IC technology lot of added features in small size.	

Example 1.1 Consider 32-bit hypothetical CPU which support 256 KB memory space, system enhanced with a word addressable memory. How many address pins are saved in enhanced CPU?

Solution :

Initial structure of memory

By default byte addressable.

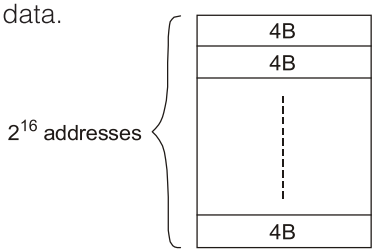


Enhanced structure of memory

Now, the system is word addressable i.e. each cell contains 4B of data.

Note that total size of memory is constant thus,

$$\text{Number of address bits} = \frac{256\ \text{KB}}{4\text{B}} = 16$$



Hence, 16 bits can uniquely determine each cell.

Therefore, number of address pins saved 18 – 16 = 2.

Example 1.2 Consider 32 bit CPU which contains 28 bit address space. What is the memory capacity in byte when CPU supports.

A. Byte addressable memory

B. Word addressable memory

Solution :

Word length of a CPU = 32 bit (or 4B)

Address space = 28 bit

A. When byte addressable memory

Memory size = 2^{28} B i.e. 256 MB

B. When word addressable memory

Memory size = $2^{28} \times 32$ bit = 1 GB

1.2 DATA STORAGE IN THE MEMORY

How to address main memory?

Main memory is a set of storage locations. Each location of memory has a unique address (a binary number starting from zero). Each "addressable" location holds a fixed number of bits. Any location can be accessed at high speed in any order (random access memory).

Student's Assignments 1

Q.1 What does CISC and RISC means?
(a) common instruction set controller and rare instruction set controller
(b) complex instruction set controller and reduced instruction set controller
(c) compiled instruction set source code and recompiled instruction source code
(d) none of the above

Q.2 A 32-bit address bus allows access to a memory of capacity
(a) 64 MB (b) 16 MB
(c) 1 GB (d) 4 GB

Q.3 The system bus is made up of
(a) data bus
(b) data bus and address bus
(c) data bus and control bus
(d) data bus, control bus and address bus

Q.4 Which of the following is not involved in a memory write operation?
(a) MAR (b) PC
(c) MDR (d) data bus

Q.5 The read/write line
(a) belongs to the data bus
(b) belongs to the control bus
(c) belongs to the address bus
(d) CPU bus

Q.6 _____ is a piece of hardware that executes a set of machine-language instructions.
(a) controller (b) bus
(c) processor (d) motherboard

Q.7 Given below are some statements associated with the registers of a CPU. Identify the false statement.
(a) The program counter holds the memory address of the instruction in execution.
(b) Only opcode is transferred to the control unit.
(c) An instruction in the instruction register consists of the opcode and the operand.
(d) The value of the program counter is incremented by 1 once its value has been read to the memory address register.

Q.8 The following are four statements about Reduced Instruction Set Computer (RISC) architectures.
1. The typical RISC machine instruction set is small, and is usually a subset of a CISC instruction set.
2. No arithmetic or logical instruction can refer to the memory directly.
3. A comparatively large number of user registers are available.
4. Instructions can be easily decoded through hard-wired control units.

Which of the above statements is true?
(a) 1 and 3 only (b) 1, 3 and 4 only
(c) 1, 2 and 3 only (d) All of these

Q.9 The word length of a CPU is defined as
(a) the maximum addressable memory size
(b) the width of a CPU register (integer or float point)
(c) the width of the address bus
(d) the number of general purpose CPU registers

Q.10 Which of the following statements is false about CISC architectures?
(a) CISC machine instructions may include complex addressing modes, which require many clock cycles to carry out.
(b) CISC control units are typically micro-programmed, allowing the instruction set to be more flexible.
(c) In the CISC instruction set, all arithmetic/logic instructions must be register based.
(d) CISC architectures may perform better in network centric applications than RISC.

Q.11 Consider a high-level language statement i – – then which addressing mode is suitable for it?
(a) autoincrement (b) indexed
(c) displacement (d) autodecrement

Q.12 In a 16-bit instruction code format 3 bit operation code, 12 bit address and 1 bit is assigned for address mode designation. How much data memory space is available
(a) 4 MB (b) 8 KB
(c) 2 KB (d) 2 GB

Q.13 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Regs[R_4] ← Regs[R_4] + Regs[R_3]
B. Regs[R_4] ← Regs[R_4] + 3
C. Regs[R_4] ← Regs[R_4] + Mem[Regs[R_1]]

List-II
1. Immediate
2. Register
3. Register indirect

Codes:

	A	B	C
(a)	3	2	1
(b)	2	1	3
(c)	1	2	3
(d)	None of these		

Q.14 Relative Addressing Mode is used to write Position-Independent code because
(a) The Code in this mode is easy to atomize
(b) The Code in this mode is easy to make resident
(c) The Code in this mode is easy to relocate in the memory
(d) Code executes faster in this mode

Q.15 Consider an (n + k) bit instruction with a k-bit opcode and single n-bit address. Then this instruction allow _____ operations and _____ addressable memory cells.
(a) 2^k, 2^{n+k} (b) 2^{n+k}, 2^{n+k}
(c) 2^k, 2^n (d) 2^{n+k}, 2^{n+1}

Q.16 The register which holds the address of the location to or from which data are to be transferred is known as
(a) index register
(b) instruction register
(c) memory address register
(d) memory data register

Q.17 Halt operation comes under _____ .
(a) data transfer (b) control transfer
(c) conversion (d) I/O transfer

Q.18 In four-address instruction format, the number of bytes required to encode an instruction is (assume each address requires 24 bits, and 1 byte is required for operation code)
(a) 9 (b) 13
(c) 14 (d) 12

Q.19 A CPU has an arithmetic unit that adds bytes and then sets its V, C and Z flag bits as follows. The V-bit is set if arithmetic overflow occurs (in 2's complement arithmetic). The C-bit is set if a carry-out is generated from the most significant bit during an operation. The Z-bit is set if the result is zero. What are the values of the V, C and Z flag bit after 8-bit byte 1100 1100 and 1000 1111 are added?

	V	C	Z
(a)	0	0	0
(b)	1	1	0
(c)	1	1	1
(d)	0	1	0

Q.20 Consider the following sequence of instructions intended for execution on a stack machine. Each arithmetic operation pops the second operand, then pops the first operand, operates on them, and then pushes the result back onto the stack

```
PUSH    b
PUSH    x
ADD
POP     c
PUSH    c
PUSH    y
ADD
PUSH    c
SUB
POP     z
```

Which of the following statements is/are true?
1. If push and pop instructions each require 5 bytes of storage, and arithmetic operations each require 1 byte of storage then the instruction sequence as a whole requires a total of 40 bytes of storage.
2. At the end of execution, z contains the same value as y.
3. At the end of execution, the stack is empty.
(a) 1 only (b) 2 only
(c) 2 and 3 only (d) 1 and 3 only

Q.21 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	List-II
A. `MOV X, R1`	1. Three-address instruction
B. `STORE X`	2. Zero-address instruction

C. `POP X`

3. One-address instruction
4. Two-address instruction

Codes:

	A	B	C
(a)	4	3	2
(b)	3	2	1
(c)	2	3	4
(d)	4	1	1

Q.22 The register which keeps track of the execution of a program and which contains the memory address of the instruction currently being executed is known as _____

(a) Index-Register
(b) Memory address register
(c) Program counter
(d) Instruction registers

Q.23 A certain processor executes the following set of machine instructions sequentially.

```
MOV R0, # 0
MOV R1, 100 (R0)
ADD R1, 200 (R0)
MOV 100 (R0), R1
```

Assuming that memory location 100 contains the value 35 (Hex), and the memory location 200 contains the value A4 (Hex), what could be said about the final result?

(a) Memory location 100 contains value A4
(b) Memory location 100 contains value DA
(c) Memory location 100 contains value D9
(d) Memory location 200 contains value 35

Answer Key:

1. (d)	**2.** (d)	**3.** (d)	**4.** (b)	**5.** (b)
6. (c)	**7.** (a)	**8.** (d)	**9.** (b)	**10.** (c)
11. (d)	**12.** (b)	**13.** (b)	**14.** (b)	**15.** (c)
16. (c)	**17.** (b)	**18.** (b)	**19.** (b)	**20.** (c)
21. (d)	**22.** (b)	**23.** (c)		

Student's Assignments Explanations

1. (d)

CISC: Complex instruction set controller
RISC: Reduced instruction set controller

2. (d)

Considering memory to be byte addressable thus, each cell is of 1B.
Number of cells = 2^{32} (because address bus contains 32 bits)
$\Rightarrow$ 2^{32} B = 4 GB

3. (d)

System bus is made up of data bus, address bus and control bus.

4. (b)

MAR is used to process address where you want to write.
MDR it will contains the data which you want to write.
Data bus it is the path through which data flows upto memory.

5. (b)

The read/write line belongs to the control bus.

6. (c)

Processor executes set of instructions.

7. (a)

(a) The program counter holds the memory address of the next instruction.
(b) Opcode determinate the control unit.
(c) IR register hold opcode.
(d) Same as (a).

8. (d)

- RISC machine instruction set is small and of fixed length.
- No arithmetic or logical instruction can refer to memory directly because it will slowdown its speed. Registers are used to perform arithmetic and logical functions.
- Large number of user registers available because there is no hindrance of costs. Speed is the main motive.
- Instructions are easily decoded since logic gates are used.

9. (b)

Word length of a CPU depends on number of data lines (or width of a CPU registers).

10. (c)

- CISC (Complex Instruction Set computers) as the name says uses complex addressing modes to enhance the performance with limited resources.
- CISC control units are typically micro-programmed. So that any changes made are easily acceptable.
- In the CISC, arithmetic or logical instructions may be memory based.

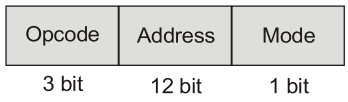
11. (d)

i – – is auto decrement instruction.

Example: store $i \rightarrow R_1$

(R_1) – will give i – –

12. (b)



Data memory space = $2^{12} \times 16$ bit

$= 2^{12} \times 2B = 8$ KB

13. (b)

(a) $R_4 \leftarrow R_4 + R_3$

Register address in mode semi, operand is directly fetched from registers.

(b) $R_4 \leftarrow R_4 + \textcircled{3}$

$\Downarrow$

Immediate value

Immediate addressing modes.

(c) $R_4 \leftarrow R_4 +$ Mem[Regs[R_1]] register indirect

14. (b)

The code is this mode is easy to relocate in the memory by using offset value.

15. (c)

- k-bit opcode means 2^k operations.
- n-bit address means 2^n addressable memory cells.

16. (c)

Memory address register is used to hold the address from which or to which data are to be transferred.

17. (b)

Halt operation comes under control transfer instruction.

18. (b)

4-address instruction format each address byte of 24 bits

$\Rightarrow$ 4-address = $24 \times 4 = 96$ bits and 1B for operation code.

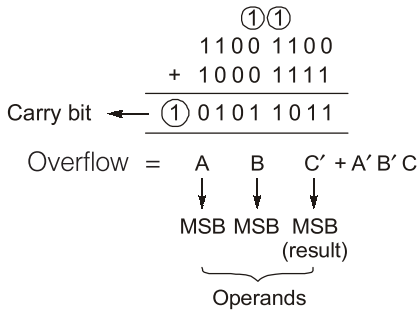
$$\text{in bytes} = \frac{96}{8} + 1 = 12 + 1 = 13 \text{ bytes}$$

19. (b)

V-bit $\Rightarrow$ overflow bit

C-bit $\Rightarrow$ carry bit

Z-bit $\Rightarrow$ zero bit



$= 111 + 000 = 1 \Rightarrow$ V-bit

And since result $\neq 0$ then Z-bit = 0

V	C	Z
1	1	0

20. (c)

```
1. PUSH   b
2. PUSH   x
3. ADD
4. POP    c
5. PUSH   c
6. PUSH   y
7. ADD
8. PUSH   c
9. SUB
10. POP   z
```

(a) Push and Pop $\rightarrow$ 5B

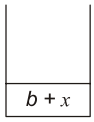
Arithmetic $\rightarrow$ 1B

Total = 7(Push/Pop) $\times$ 5B + 3(arithmetic) $\times$ 1

$= 35 + 3 = 38$B

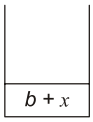
Hence, 1 statement is false.

(b) After executing 1, 2, 3

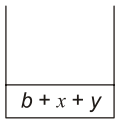


Pop $c \Rightarrow c = b + x$

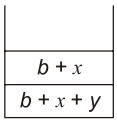
Push $c \Rightarrow$



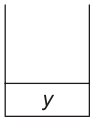
After executing 6, 7



Push $c \Rightarrow$



Sub



$\leftarrow b + x + y - b - x = y$

Pop $z \Rightarrow$ $\boxed{z = y}$ and stack is empty.

21. (d)

A. `MOV X, R1` → Two address instruction

B. `STORE X` → One address instruction

C. `POP X` → One address instruction

It Pops out top of stack and store it in X location.

22. (b)

MAR, (already explained previously).
Current execution information in MAR.

23. (c)

1. `MOV R0, # 0`
2. `MOV R1, 100 (R0)` — 100: $(35)_{16}$
3. `ADD R1, 200 (R0)`
4. `MOV 100 (R0), R1` — 200: $(A4)_{16}$

After (1) R_0 0

After (2) $R_1 \leftarrow M[100 + R_0]$

$R_1 \leftarrow (35)_{16}$

After (3) $R_1 \leftarrow R_1 + M[200 + R_0]$

```
  3 5
  A 4
R1 ← D 9
```

After (4) `M[200 + R0] ← R1` — 100: D9

`M[100] ← D9` — 200: A4

Option (c) is correct.

Student's Assignments 2

Q.1 A PC relative mode branch instruction is 5 B long. The address of the instruction in decimal is 238715. The branch target address if the signed displacement is –32 is _____.

Q.2 Consider the following program segment:

	Instruction	Meaning	Instruction size (in word)
I_1	Load r_0, 300	$r_0 \leftarrow$ [300]	2
I_2	MOV r_1, 5000	$r_1 \leftarrow$ Mem [5000]	2
I_3	MOV r_2, (r_1)	$r_2 \leftarrow$ Mem [r_1]	1
I_4	Add r_0, r_2	$r_0 \leftarrow r_0 + r_2$	1
I_5	MOV, 6000, r_0	Mem [6000] $\leftarrow r_0$	2
I_6	HALT	Machine Halts	1

Consider that the memory is byte addressable with word size 16 bits and the program has been loaded starting from memory location $(2000)_{10}$. The return address will be saved in the stack, if an interrupt occurs while the CPU has been halted after executing the HALT instruction is _____.

Q.3 Match **List-I** (Addressing Mode) with **List-II** (Location of operand) and select the correct answer:

List-I

A. Implied
B. Immediate
C. Register
D. Register Indirect

List-II

1. Registers which are in CPU
2. Register specifies the address of the operand.

3. Specified in the address field of an instruction
4. Specified implicitly in the definition of instruction

Codes:

	A	B	C	D
(a)	4	3	1	2
(b)	4	1	3	2
(c)	4	2	1	3
(d)	4	3	2	1

Q.4 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. To access constant value
B. Global variable
C. Pointer
D. Array

List-II

1. Indirect addressing mode
2. Direct addressing mode
3. Based index addressing mode
4. Immediate addressing mode

Codes:

	A	B	C	D
(a)	1	2	3	4
(b)	2	3	4	1
(c)	4	2	1	3
(d)	2	3	1	4

Q.5 Consider we have the following values in the given memory locations:

Location	Value
1000	1300
1100	1200
1200	800
1300	1200

Consider that the index register R1 store 200 and is always implicitly used for the indexed addressing mode. What datum is loaded into the accumulator if the instruction is "LOAD 1000" for direct addressing mode, indirect addressing mode and base (indexed) addressing modes respectively.

(a) 1200, 800, 1100 (b) 1200, 800, 1300
(c) 1100, 1200, 800 (d) 1300, 1200, 800

Q.6 A device with data transfer rate of 20 KBps is connected to a CPU byte wise. Assume byte transfer time between the device and CPU is negligible and interrupt overhead is 20 μsec. The performance gain under interrupt mode over program controlled mode is _____.

Q.7 Consider the following program segment:

	Instruction	Meaning	Size (words)
I_1	LOAD r_0, 500	$r_0 \leftarrow [500]$	2
I_2	MOV r_1, r_0	$r_1 \leftarrow [r_0]$	1
I_3	ADD r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_4	INC r_0	$r_0 \leftarrow r_0 + 1$	1
I_5	INC r_1	$r_1 \leftarrow r_1 + 1$	1
I_6	ADD r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_7	Store r_1, r_0	$M[(r_1)] \leftarrow r_0$	2
I_8	Halt	Stop	1

Assume that memory is word addressable with word size 32 bits. Program is loaded into memory location $(3001)_{10}$ onwards. The value of PC at the end of execution of above program is _____.

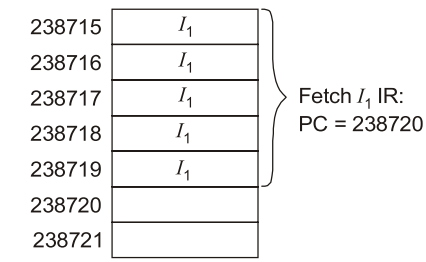
Q.8 Assume that five instructions of the loop body starting memory locations are 1000, 1004, 1008, 1012 and 1016 respectively. Assume each instruction takes 4 bytes of memory. The offset needed to return to the loop are _____.

Answer Key:

1. (238688) **2.** (2016) **3.** (a) **4.** (c) **5.** (d)
6. (2.5) **7.** (3010) **8.** (– 20)

Student's Assignments — Explanations

1. (238688)



Effective address = PC + Relative value
= 238720 + (–32) = 238688

2. (2016)

	Instruction	Instruction size	Location
I_1	Load r_0, 300	2 word	2000-2003
I_2	MOV r_1, 5000	2 word	2004-2007
I_3	MOV r_2, (r_1)	1 word	2008-2009
I_4	Add r_0, r_2	1 word	2010-2011
I_5	MOV, 6000, r_0	2 word	2012-2015
I_6	HALT	1 word	2016-2017

$\therefore$ Since 1 word is of 2 bytes.

If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address 2016 is saved in the stack.

3. (a)

- **Implied addressing mode:** Specified implicitly in the definition of instruction.
- **Immediate addressing mode:** Specified in the address field of an instruction.
- **Register addressing mode:** Registers which are in CPU.
- **Register indirect addressing mode:** Register specifies the address of the operand.

4. (c)

- To access constant value Immediate addressing mode is used.
- Global variable are using Direct addressing mode.
- Pointer are implemented using Indirect addressing mode.
- Array are implemented using Based index addressing mode.

5. (d)

Instruction : "Load 1000"

Direct Addressing Mode: Since the content of location '1000' is '1300'. Hence, 1300 will be loaded.

Indirect Addressing Mode: The content of location '1000' is '1300'. The content of memory location '1300' is '1200'. Hence, 1200 will be loaded.

Base (Indexed) Addressing Mode: [1000 + 200] $\Rightarrow$ [1200]. The content of memory location '1200' is 800.

6. (2.5)

20 KB — 1 sec

1 B — ?

$$\text{Transfer time of 1 byte} = \frac{1}{20\text{ K}} = 0.05\text{ ms}$$

$$ET_{\text{Prog. I/O}} = 0.05\text{ ms}$$
$$ET_{\text{INT - I/O}} = 20\,\mu\text{sec}$$

$$\text{Performance gain} = \frac{ET_{\text{Prog. I/O}}}{\text{ET - I/O}} = \frac{0.05\text{ ms}}{20\,\mu\text{sec}} = 2.5$$

7. (3010)

Word addressable storage:

3001 – 3002 $\rightarrow I_1$
3003 $\rightarrow I_2$
3004 $\rightarrow I_3$
3005 $\rightarrow I_4$
3006 $\rightarrow I_5$
3007 $\rightarrow I_6$
3008 – 3009 $\rightarrow I_7$
3010 $\rightarrow I_8$

Valid program counter value after program is 3010.

8. (–20)

Suppose 5 instructions are I_1, I_2, I_3, I_4 and I_5.

PC value at the end of loop = 1020

Offset = – 20