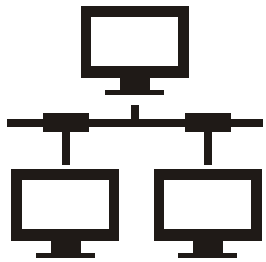
COMPUTER SCIENCE & IT



POSTAL
BOOK PACKAGE
2024

OBJECTIVE PRACTICE SETS

MADE EASY Publications

www.madeeasypublications.org

POSTAL BOOK PACKAGE 2024

CONTENTS

COMPUTER SCIENCE & IT

Computer Organization & Architecture

1 CHAPTER
Basics of Computer Design

Multiple Choice Questions & NAT Questions

Q.1 The computer performs all mathematical and logical operations inside its
(a) Memory unit (b) Central processing unit
(c) Output unit (d) Visual display unit

Q.2 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Pointer
B. Position Independent code
C. Constant operand

List-II
1. Indirect AM
2. Immediate AM
3. Relative AM

Code:

	A	B	C
(a)	1	2	3
(b)	3	2	1
(c)	1	3	2
(d)	2	3	1

Q.3 The most appropriate matching of the following pairs is

Column 1	Column 2
X: Indirect addressing	1. Loops
Y: Immediate addressing	2. Pointers
Z: Auto-decrement address	3. Constant

(a) X-2, Y-3, Z-1 (b) X-3, Y-2, Z-1
(c) X-1, Y-3, Z-2 (d) X-3, Y-1, Z-2

Q.4 Consider the following I/O instruction format for IBM 370 I/O channel

Operation Code	Channel Address	Device Address

Then operation code specifies
1. Test I/O
2. Test channel
3. Store channel identification
4. Halt device

(a) Only 1 and 4 (b) Only 2 and 3
(c) 1, 2, 3 and 4 (d) Only 1, 3 and 4

Q.5 An interrupt that can be temporarily ignored by the counter is known as
(a) Vectored interrupt
(b) Non-maskable interrupt
(c) Maskable interrupt
(d) Low priority interrupt

Q.6 A processor can support a maximum memory of 4 GB where memory is word addressable and word is 2 bytes. What will be the size of the address bus of the processor?
(a) At least 2 bytes (b) At least 28 bits
(c) At least 31 bits (d) Minimum 4 bytes

Q.7 A digital computer has memory unit with 24 bits word. The instruction set consists of 150 different operations. All instructions have an operation code part and an address part. Each instruction is stored in one word of memory. How many bits are needed for the OPCODE and how many bits are left for the address of the instruction.
(a) 8, 16 (b) 16, 64
(c) 4, 8 (d) 8, 64

Q.8 An instruction is stored at location 300 with its address field. At location 301 the address field has value 400. A processor register R1 contains the number 200. Evaluate the effective address matching the following addressing modes to their respective addresses.

A. Direct	1. 702
B. Immediate	2. 200
C. Relative	3. 400
D. Register indirect	4. 600
E. Index (R1 is index)	5. 301

(a) A3 B5 D2 E4 C1 (b) A3 B4 C1 D1 E5
(c) A5 B3 C2 D1 E4 (d) A4 B3 C1 D5 E2

Q.9 What is the most appropriate match for the items in the first column with the items in the second column:

Column 1:

X. Indirect addressing
Y. Indexed addressing
Z. Base register addressing

Column 2:

1. Array implementation
2. Writing relocatable code
3. Passing array as parameter

(a) X-3, Y-1, Z-2 (b) X-2, Y-3, Z-1
(c) X-3, Y-2, Z-1 (d) X-1, Y-3, Z-2

Q.10 In which of the following address mode, the content of the program counter is added to the address part of the instruction to get the effective address?

(a) Indexed addressing mode
(b) Implied addressing mode
(c) Relative addressing mode
(d) Register addressing mode

Q.11 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I

A. Stack overflow
B. Supervisor call
C. Invalid opcode
D. Timer

List-II

1. Software interrupt
2. Internal interrupt
3. External interrupt
4. Machine check interrupt

Codes:

	A	B	C	D
(a)	2	3	4	1
(b)	2	1	2	3
(c)	3	1	2	4
(d)	3	1	4	2

Q.12 In a certain processor, a 2 byte Jump instruction is encountered at memory address 3010H, the Jump instruction is in PC relative mode. The instruction is JMP – 7 where – 7 is signed byte. Determine the Branch Target Address

(a) 300B H (b) 3009 H
(c) 3003 H (d) 3007 H

Q.13 Processor *XYZ* supports only the immediate and the direct addressing modes. Which of the following programming language data structures cannot be implemented on this processors?

1. Pointers
2. Arrays
3. Records

(a) 1, 2 and 3 (b) 2 and 3
(c) 1 and 2 (d) Only 1

Q.14 Word 20 contains 40
Word 30 contains 50
Word 40 contains 60
Word 50 contains 70

Which of the following instructions loads 60 into the accumulator?

(a) Load immediate 20
(b) Load direct 30
(c) Load indirect 20
(d) Load indirect 30

Q.15 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I	**List-II**
A. $A[1] = B[J]$;	1. Indirect addressing
B. while [$*A$++];	2. Indexed addressing
C. int temp = $*x$;	3. Auto increment

Codes:

	A	B	C
(a)	3	2	1
(b)	1	3	2
(c)	2	3	1
(d)	1	2	3

Q.16 In immediate addressing mode, where is the operand placed?

(a) In memory
(b) In stack
(c) In CPU register
(d) In instruction after opcode

Q.17 If the last operand performed on a computer with an 8-bit word has an addition in which the two operands were 00000010 and 00000011, what would be value of the overflow, sign and half-carry flags respectively?

(a) 0, 1, 0 (b) 0, 1, 1
(c) 1, 0, 1 (d) 0, 0, 0

Q.18 A 4-byte long PC-relative branch instruction is fetched from memory address $(512)_{10}$ and while its execution, the branch is made to location $(885)_{10}$. What is unsigned displacement present in the instruction? (Relative value) _____?

Q.19 A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____.

Q.20 The register which contains the data to be written into or read out of the addressed location is known as
(a) Memory address register
(b) Memory data register
(c) Program computer
(d) Index register

Q.21 In four-address instruction format, the number of bytes required to encode an instruction is (assume each address requires 24 bits and 1 byte is required for operation code)
(a) 9 (b) 13
(c) 14 (d) 12

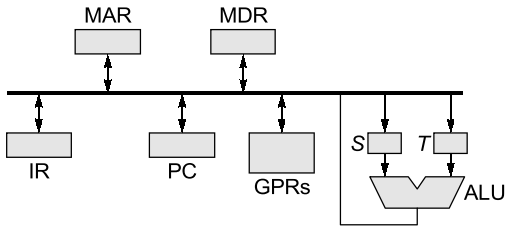
Q.22 The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

MOVI Rs, 1;	Move immediate
LOAD Rd, 1000(Rs);	Load from memory
ADDI Rd, 1000;	Add immediate
STOREI 0(Rd), 20;	Store immediate

Which of the statements below is TRUE after the program is executed?
(a) memory location 1000 has value 20
(b) memory location 1020 has value 20
(c) memory location 1021 has value 20
(d) memory location 1001 has value 20

Q.23. A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?
(a) 400 (b) 500
(c) 600 (d) 700

Q.24 Consider the following data path of a CPU:



The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycle are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory but into the MDR.

The instruction "add R_0, R_1" has the register transfer interpretation $R_0 <= R_0 + R_1$. The minimum number of clock cycles needed for execution cycle of this instruction is
(a) 2 (b) 3
(c) 4 (d) 5

Q.25 In the previous question the instruction "call *Rn*, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is
Rn < = PC + 1;
PC < = *M* [PC];
The minimum number of CPU clock cycles needed during the execution cycle of this instruction is
(a) 2 (b) 3
(c) 4 (d) 5

Q.26 Consider the following program segment:

	Instruction	Meaning	Size (words)
I_1	LOAD r_0, 500	r_0 – [500]	2
I_2	MOV r_1, r_0	$r_0 - r_0$	1
I_3	Add r_0, r_1	$r_0 - r_0 + r_1$	1
I_4	Inc r_0	$r_0 - r_0 + 1$	1
I_5	Inc r_1	$r_1 - r_1 + 1$	1
I_6	Add r_0, r_1	$r_0 - r_0 + r_1$	1
I_7	Store r_1, r_0	M[(r_1)r_0]	2
I_8	Halt	Stop	1

Assume that memory is word addressable with word size 32 bits. Program is loaded into memory location 3000 onwards. The value of PC at the end of execution of above program is _____.

Q.27 A computer has 32 bit instruction and 9-bit address. If there are 400 two address instructions then how many one address instructions can be formulated?

(a) 2^{14} (b) $2^{32} - 200$
(c) $2^{14} - 400$ (d) $(2^{14} - 400) \times 2^9$

Q.28 In which addressing mode, the effective address of the operand is generated by adding a constant value to the content of a register?

(a) Absolute mode (b) Indirect mode
(c) Immediate mode (d) Index mode

Q.29 A complier designer has to decide between two code sequences for a particular m/c. Here data shown below. So which of the code sequence is faster?

Instruction (log)	CPI
A	1
B	2
C	3

Code sequence	Instruction count		
	A	B	C
1	2	1	2
2	4	1	1

(a) Code sequence 1 is faster
(b) Code sequence 2 is faster
(c) Both are same
(d) None of these

Q.30 Consider a 16-bit processor in which the following one address Instruction appeals in main memory starting at location 200.

200	Opcode
201	500
202	Next Instruction
⋮	
500	999

There is also a base register that contains the value 100.

Match **List-I** (Mode) with **List-II** (Effective Address) and select the correct answer using the codes given below the lists:

List-I	List-II
A. Immediate	1. 600
B. Direct	2. 999
C. Memory Indirect	3. 201
D. PC-relative	4. 500
E. Base-register	5. 702

Codes:

	A	B	C	D	E
(a)	3	5	2	4	1
(b)	4	5	2	1	3
(c)	3	4	2	5	1
(d)	3	4	5	1	2

Q.31 The control word of micro programmed control is as follows:

condition	control field	next address

It has to generate 48 control signals, next addresses are selected based on 16 conditional or flag information. The control memory has 84 control programs of size 8 words.

What is the size (in bits) of control word in horizontal micro-programming? _____

Q.32 Most relevant addressing mode to write position independent code is

(a) direct (b) indirect
(c) relative (d) indexed mode

Q.33 Consider the following program segment. Here *R*1, *R*2 and *R*3 are the general purpose registers.

Instruction	Operation	Instruction Size (no. of words)
MOV *R*1, 3000	*R*1 ← *M*[3000]	2
Loop:		
MOV *R*2,(*R*1)	*R*2 ← *M*[*R*3]	1
ADD *R*2, *R*1	*R*2 ← *R*1 + *R*2	1
MOV (*R*3), *R*2	*M*(*R*3] ← *R*2	1
INC *R*3	*R*3 ← *R*3 + 1	1
DEC *R*1	*R*1 ← *R*1 – 1	1
BNZ LOOP	Branch on not zero	2
Halt	Stop	1

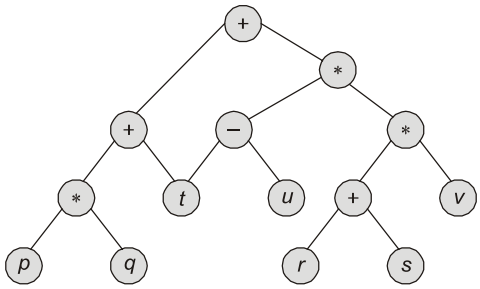
Assume that the content of memory location 3000 is 10 and the content of the register *R*3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 100. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

(a) 10 (b) 11
(c) 20 (d) 21

Q.34 Consider a processor with byte-addressable memory. Assume that all registers, including Program Counter (PC) and Program Status Word

in memory. The binary operators used in the tree can be evaluated by the machine only when all operands are in register. The instruction produce result only in a register.



What is the minimum number of registers needed to evaluate the expression if, no intermediate results can be stored in memory?

(a) 3 (b) 4
(c) 5 (d) 6

■■■■

Answers Basics of Computer Design

1.	(b)	2.	(c)	3.	(a)	4.	(c)	5.	(c)	6.	(c)	7.	(a)	8.	(a)	9.	(a)
10.	(c)	11.	(b)	12.	(a)	13.	(c)	14.	(c)	15.	(c)	16.	(d)	17.	(d)	18.	(369)
19.	(16383)	20.	(b)	21.	(b)	22.	(d)	23.	(c)	24.	(b)	25.	(b)	26.	(3009)	27.	(d)
28.	(d)	29.	(b)	30.	(c)	31.	(62)	32.	(c)	33.	(d)	34.	(d)	35.	(b)	36.	(c)
37.	(b)	38.	(c)	39.	(d)	40.	(b)	41.	(c)	42.	(b)	43.	(c)	44.	(d)	45.	(d)
46.	(c)	47.	(c)	48.	(a)	49.	(a)	50.	(c)	51.	(a)	52.	(c)	53.	(b)	54.	(a)
55.	(–128)	56.	(a)	57.	(a)	58.	(b)	59.	(d)	60.	(a)	61.	(d)	62.	(16)	63.	(d)
64.	(b)	65.	(c)	66.	(a)	67.	(d)	68.	(92)	69.	(2032)	70.	(c)	71.	(a)	72.	(b)
73.	(c)	74.	(b)	75.	(c)	76.	(2048)	77.	(d)	78.	(a, b, d)	79.	(c)	80.	(b, c)		
81.	(a, c)	82.	(b, c)	83.	(b)												

Explanations Basics of Computer Design

2. (c)

For making use of pointer in programs, indirect addressing mode is used.

Pointer stores the address of a variable and indirect addressing mode stores address of effective address the instruction.

Position independent code make use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.

Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

4. (c)

The operation code specifies one of eight input output instructions: Start input/output, start input/output fast release, test input/output, clear input/output, halt input/output, halt device, test channel and store channel identification.

5. (c)

Maskable interrupt temporally ignored by counter.

6. (c)

$$\text{Memory size} = 4\text{ GB} = 2^{32}\text{ B}$$
$$\text{Word size} = 2\text{ B}$$

$$\text{So, unique address} = \frac{2^{32}}{2^{1}} = 2^{31}$$

Hence, atleast 31 bits are required.

7. (a)

Each instruction is stored in one word of memory. Memory is word addressable and 1 word = 24 bits ⇒ 3 bytes.

Total number bits = 24

The instruction set consists of 150 different operations. To generate 150 different operations we need minimum 8 bits are required.

OP code	Address
8	16

So, option (a) is correct.

8. (a)

For direct, EA = address field value in IR (instruction register) = 400

For immediate, actually no meaning of effective address. So, EA here will be just the address of the operand field which is otherwise address field = 301.

For relative addressing, we have EA = PC value (current) + Address field value

EA = 302 + 400 = 702

For register indirect, the EA is the content of the register, the register name being present in the address field of instruction.

So, EA = content of R1 = 200

For indexed mode = Base address + index register content

= 400 + 200 = 600

So, option (a) is correct.

10. (c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

So, option (c) is correct.

11. (b)

- Stack over flow is a internal interrupt.
- Supervisor call is a software interrupt.
- Invalid opcode is a internal interrupt.
- Timer is a external interrupt.

12. (a)

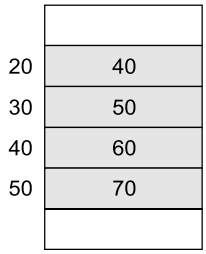
The Jump instruction is at address 3010 H and instruction is 2 bytes. Therefore, PC points to 3012 H on execution of this instruction.

Now Branch Target PC = PC + (–7)

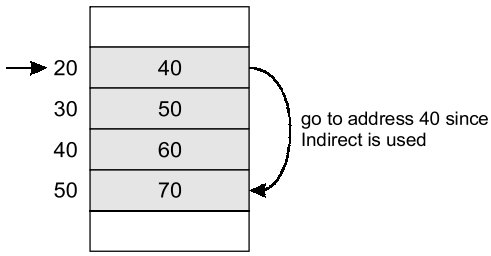
= 3012 H – 7 H = 300 BH

14. (c)

The given information can be understood as



Now load indirect 20 will load 60 into as follows



Hence (c) is correct option.

16. (d)

In immediate addressing mode, the operand is specified in the instruction itself.

For example: MOV R1, 12H is the immediate AM with 12 is operand.

17. (d)

$$\begin{array}{r} 00000010 \\ 00000011 \\ \hline 00000101 \end{array}$$

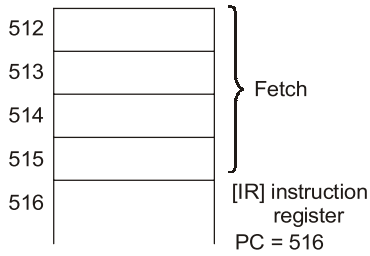
Overflow = 0, sign = 0, half carry = 0

Half carry indicate addition of pack at decimal numbers. When carry takes out of the lower digit order, this flag is set.

Auxiliary carry is also known as half carry.

18. (369)

4 byte instruction storage



Effective address = PC + Relative value

Relative value = EA – PC

= 885 – 516 = (369)10

So, answer is 369.