POSTAL Book Package 2022

Electrical Engineering

Objective Practice Sets

Computer Fundamentals

Contents

MADE EASY Publications

1 CHAPTER
Memory Organization and IO Organization

Q.1 More than one word are put in one cache block to
(a) Exploit the temporal locality of reference in a program.
(b) Exploit the spatial locality of reference in a program.
(c) Reduce the miss penalty.
(d) None of the above

Q.2 The access time of a word in a 4 MB main memory is 100 ns. The access time of a word in a 32 kB data cache memory is 10 ns. The average data cache hit ratio is 0.95. The effective memory access time is
(a) 9.5 ns (b) 15 ns
(c) 20 ns (d) 50 ns

Q.3 A memory system of size 128 K bits is required to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is
(a) 64 (b) 4
(c) 8 (d) 16

Q.4 A processor can support a maximum memory of 4 GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at least
(a) 32 bits (b) 31 bits
(c) 35 bits (d) 34 bits

Q.5 For the daisy chain scheme of connecting I/O devices, which of the following statements is true?
(a) It gives non-uniform priority to various devices.
(b) It gives uniform priority to all devices.
(c) It is only useful for connecting slow devices to a processor.
(d) It requires a separate interrupt pin on the processor for each device.

Q.6 The main memory of a computer has 2 cm blocks while the cache has 2 c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set
(a) (k mod m) of the cache
(b) (k mod c) of the cache
(c) (k mod 2 c) of the cache
(d) (k mod 2 cm) of the cache

Q.7 When an interrupt occurs, an operating system
(a) ignores the interrupt
(b) always changes state of interrupted process after processing the interrupt
(c) always resumes execution of interrupted process after processing the interrupt
(d) may change state of interrupted process to 'blocked' and schedule another process

Q.8 A system uses FIFO policy for page replacement. It has 4 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur?
(a) 196 (b) 192
(c) 197 (d) 195

Q.9 If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?
(a) Width of tag comparator
(b) Width of set index decoder
(c) Width of way selection multiplexor
(d) Width of processor to main memory data bus

Q.10 According to temporal locality, processes are likely to reference pages that
(a) have been referenced recently.
(b) are located at address near recently referenced pages in memory.
(c) have been preloaded in memory.
(d) None of these

Q.11 A system which has a lot of crashes, data should be written to the disk, using
(a) Write – through
(b) Write – back
(c) Any one from (a) and (b)
(c) Some other techniques are required and none of the above can do this.

Q.12 The principle of locality justifies the use of
(a) Interrupts (b) Threads
(c) DMA (d) Cache Memory

Q.13 Consider a system with 2 level cache. Access times of level 1 cache, level 2 cache and main memory are 1 ns, 10 ns and 500 ns respectively. The hit rates of level 1 and level 2 caches are 0.8 and 0.9 respectively. What is the average access time of the system ignoring the search time within the cache?
(a) 13.0 (b) 12.8
(c) 12.6 (d) 12.4

Q.14 Consider a memory system with the following parameters :

T_c = Cache Access Time
= 100 ns
T_m = Main Memory Access Time
= 1200 ns

If we would like to have effective (average) memory access time to be or more than 20% higher than cache access time, the hit ratio for the cache must at least be :
(a) 80% (b) 90%
(c) 98% (d) 99%

Q.15 A disc drive has an average seek time of 10 ms, 32 sectors on each track and 512 bytes per sector. If the average time to read 8 kbytes of continuously stored data is 20 ms, what is the rotational speed of the disc drive?
(a) 3600 rpm (b) 6000 rpm
(c) 3000 rpm (d) 2400 rpm

Q.16 In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is
(a) Non-maskable and non-vectored
(b) Maskable and non-vectored
(c) Non-maskable and vectored
(d) Maskable and vectored

Q.17 The access time of a cache memory is 100 ns and that of main memory is 1 μs. 80% of the memory requests are for read and others are for write. Hit ratio for read only accesses is 0.9. A write through procedure is used. The average access time of the system for both read and write requests is
(a) 200 ns (b) 360 ns
(c) 720 ns (d) 1100 ns

Q.18 A computer system has a 4 K word cache organized in block-set associative manner with 4 blocks per set, 64 words per block. The numbers of bits in the SET and WORD fields of the main memory address formula are respectively
(a) 15 and 4 (b) 6 and 4
(c) 7 and 2 (d) 4 and 6

Q.19 Which of the following requires a device driver?
(a) Register (b) Cache
(c) Main memory (d) Disk

Q.20 A disk pack contains 6 disks. Data can be read/written from both the surfaces of the disk. There are 200 tracks on each disk surface, each track is divided into 50 sectors and each sector contains 512 B. What is the total storage capacity of the disk pack (in bytes)?
(a) $512 \times 50 \times 200 \times 12$
(b) $512 \times 50 \times 200 \times 20$
(c) $512 \times 50 \times 200 \times 6$
(d) $\dfrac{512 \times 50 \times 200 \times 6}{2}$

Q.21 Which of the following semiconductor memory is used for cache memory?
(a) SRAM (b) DRAM
(c) ROM (d) PROM

Q.22 In a cache with 64-byte cache lines, how many bits are used to determine which byte within a cache line an address points to?
(a) 16 (b) 8
(c) 6 (d) 3

Q.23 Consider a system that uses interrupt driven I/O for a particular device which has an average data transfer rate of 8 kbps. The processing of the interrupt which includes the time to jump to ISR, its execution and returning to the main program is 100 μs. What fraction of processor time consume by the device, if the device interrupts for every 1 byte (in %)?

(a) 80 (b) 40
(c) 20 (d) 100

Q.24 The write through procedure is used
(a) To write on the memory directly.
(b) To write and read from memory simultaneously.
(c) To write directly on the memory and cache whenever a hit occurs on a cache.
(d) None of the above.

Q.25 The fastest data access is provided using
(a) Caches (b) DRAM's
(c) SRAM's (d) Registers

Q.26 Consider the following statements:
1. The processor interrupts the program currently being executed.
2. The action requested by the interrupt is performed by the ISR.
3. Interrupts are enabled and execution of the interrupted program is resumed.
4. The device raises an interrupt request.
5. The device is informed that its request has been recognized and in response, it deactivates the interrupt request signal.

Arrange the above statements meaningfully, then what should be the sequence?
(a) 4, 5, 1, 2, 3 (b) 4, 1, 5, 2, 3
(c) 2, 4, 5, 1, 3 (d) 4, 5, 1, 3, 2

Q.27 Consider cache memory with hit ratio for read and write as 70% and 80%. Access time of a cache memory is 50 ns/word and main memory access time is 200 ns/word. When there is a miss operation then 4 words block is transferred from main memory to cache memory. Suppose system generated 30% write request and 70% read request. Find efficiency (in million words per) for a write through cache.
(a) 2.3 (b) 3.3
(c) 4.3 (d) 5.3

Q.28 The minimum time delay between the initiations of two independent memory operations is called
(a) Access Time (b) Cycle Time
(c) Transfer Time (d) Latency Time

Q.29 Which of the following statement(s) is/are true?
Statement 1 : The main advantage of direct mapping is that the cache hit ratio increases drastically if two or more frequently used blocks map onto same region.
Statement 2 : For two-level memory hierarchy cache and main memory, WRITE THROUGH results in more write cycles to main memory than WRITE BACK.
(a) Only S1 (b) Only S2
(c) Only S1 and S2 (d) None of these

Q.30 A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?
(a) 10 (b) 6.4
(c) 1 (d) 0.64

Q.31 A cache contains n blocks and main memory contains m blocks. If k-way set associative mapping is used then what will be number of TAG bits.
(a) $\log_2 \frac{mk}{n}$ (b) $\log_2 \frac{m}{n}$
(c) $\log_2 \frac{nk}{m}$ (d) $\log_2 \frac{mn}{k}$

Q.32 Which of the following statements are true?
1. Update bit is used in the write back cache to indicate the cache updation.
2. In hierarchical memory access organization CPU perform read and write operation on only level 1 memory.
3. In simultaneous memory access organization CPU perform read and write operation on any level of memory.

(a) 1 and 2 only (b) 1 and 3 only
(c) 2 and 3 only (d) 1, 2 and 3 only

Q.33 Which of the following is true?
(a) In write through protocol, cache location and main memory location are updated simultaneously.
(b) In write back protocol, cache location and main memory location are updated simultaneously.
(c) Modified or dirty bits are used by write through protocol.
(d) None of these

Q.34 In a vectored interrupt :
(a) the interrupting device supplies the branch information to the processor through an interrupt vector.
(b) the CPU does not know, which device cause the interrupt without polling each I/O interface.

Q.44 **Statement (I):** Most personal computers use static RAMs for their main memory.
Statement (II): Static RAMs are much faster than dynamic RAMs.

Q.45 **Statement (I):** Associative memory is fast memory.
Statement (II): Associative memory searches by content and not by accessing of address.

■■■■

Answers Memory Organization and IO Organization

1. (b)	2. (b)	3. (c)	4. (b)	5. (a)	6. (b)	7. (d)	8. (a)	9. (d)
10. (a)	11. (a)	12. (d)	13. (a)	14. (b)	15. (b)	16. (d)	17. (b)	18. (d)
19. (d)	20. (a)	21. (a)	22. (c)	23. (a)	24. (c)	25. (d)	26. (b)	27. (b)
28. (b)	29. (b)	30. (c)	31. (a)	32. (d)	33. (a)	34. (a)	35. (b)	36. (d)
37. (c)	38. (b)	39. (b)	40. (d)	41. (a)	42. (a)	43. (d)	44. (d)	45. (a)

Explanations Memory Organization and IO Organization

1. (b)

Spatial Locality : If a particular storage location is referenced at a particular time, then it is likely that nearby memory locations will be referenced in the near future. Thus keeping more than one block helps in using spatial locality concept.

2. (b)

Hit ratio, $H_c = 0.95$

Cache Memory Access Time

$T_c = 10$ ns

Main Memory Access Time

$T_m = 100$ ns

$EAT = H_c(T_c) + (1 - H_c)(T_c + T_m)$

$EAT = 0.95 \times 10 + 0.05 \times 110$

$EAT = 9.5 + 5.5$

$EAT = 15$ ns

3. (c)

Size of chip $= 2^{12} \times 4$ bits

Size of memory $= 128$ k bits

$$\text{Number of chips} = \frac{2^7 \times 2^{10}}{2^{12} \times 2^2} = 8$$

4. (b)

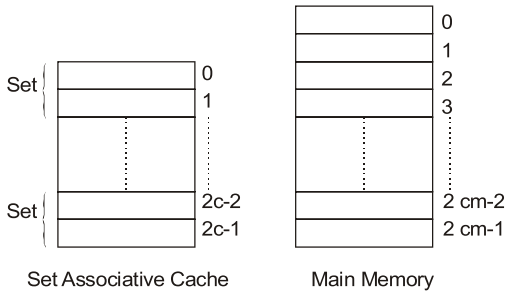
Total number of memory words (or) total number of memory addresses $= \frac{4 \times 2^{30}}{2} = 2 \times 2^{30} = 2^{31}$.

To represent 2^{31} addresses, at least 31 address lines are required.

5. (a)

The daisy-chaining method of establishing priority consists of a serial connection of all devices that request an interrupt. The device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the chain. The farther the device is from the first position, the lower is its priority. Therefore daisy-chain gives non-uniform priority to various devices.

6. (b)



Number of set in set associative cache

$$= \frac{\text{number of blocks in cache}}{\text{number of blocks in one set}} = \frac{2c}{2} = c$$

Number of sets in cache = c

Therefore, the block k of the main memory maps to the set (k mod c) of the cache.

7. (d)

An interrupt is a signal from a device attached to a computer or from a program within the computer